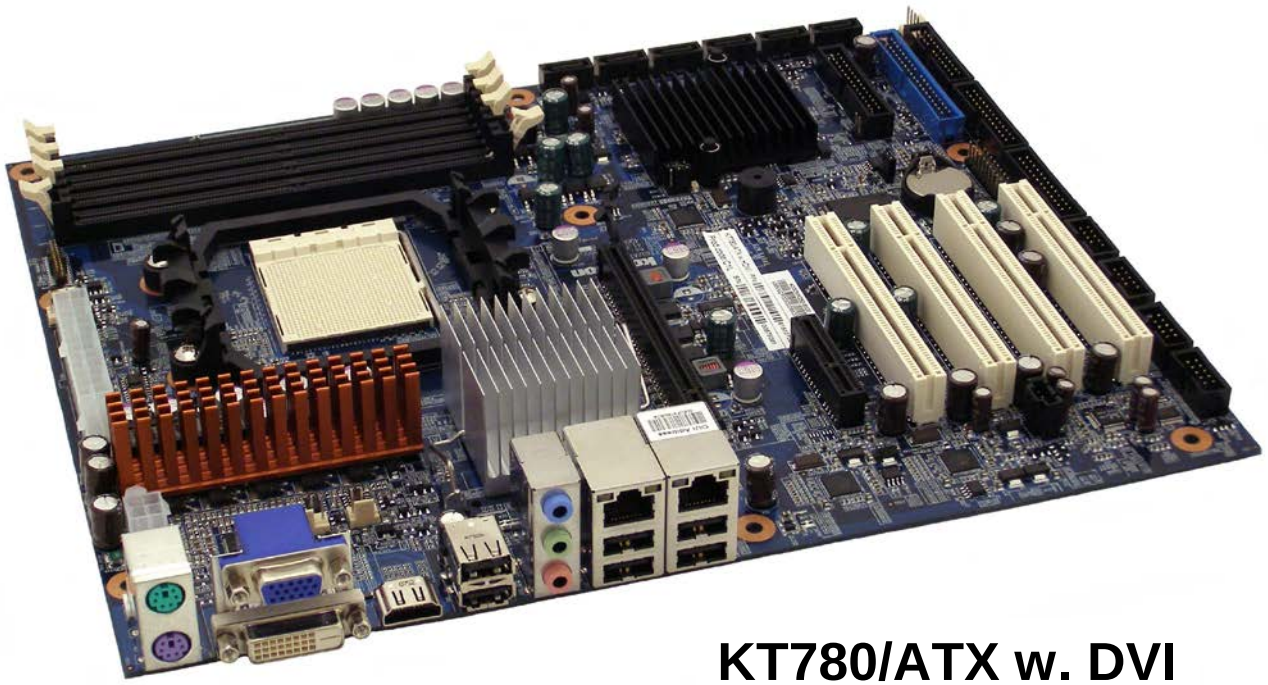
User Manual

for the Motherboards:



KT780/ATX w. DVI

KT780/ATX w. HDMI

Document revision history.

Revision	Date	By	Comment
D	Jan. 10th 2012	MLA	Added “mounting the board to chassis”. Revision of processor support table.
C	Oct 1st 2009	MLA	Correction to LAN connector pinning. Battery alternative added. Minor corrections. BIOS updated (added Default Boot Order, ECC and RTC).
B	Oct 28th 2008	JS/MLA	Minor additional information
A	Sep 18th 2008	JS	Revised, BIOS features added
0	May 26th 2008	JS	First preliminary manual version.

Life Support Policy

KONTRON Technology's PRODUCTS ARE NOT FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT EXPRESS WRITTEN APPROVAL OF THE GENERAL MANAGER OF KONTRON Technology A/S.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

KONTRON Technology Technical Support and Services

If you have questions about installing or using your KONTRON Technology Product, check this User's Manual first – you will find answers to most questions here. To obtain support, please contact your local Distributor or Field Application Engineer (FAE).

Before Contacting Support: Please be prepared to provide as much information as possible:

- CPU Board
  1. Type.
  2. Part-number.
  3. Serial Number.
- Configuration
  1. CPU Type, Clock speed.
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup).
  4. BIOS Settings different than *Default* Settings (Refer to the BIOS Setup Section).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

Table of contents:

1. Introduction

This manual describes the KT780/ATX w. DVI and KT780/ATX w. HDMI boards made by KONTRON Technology A/S. The boards will also be denoted KT780 family if no differentiation is required.

All boards are to be used with the AMD Phenom ™, AMD Athlon X2 64 ™, AMD Athlon X2 ™, and Sempron AM2/AM2+ socket.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KT780 Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in chapter 3 before switching-on the power.

2. Installation procedure

2.1 Installing the board

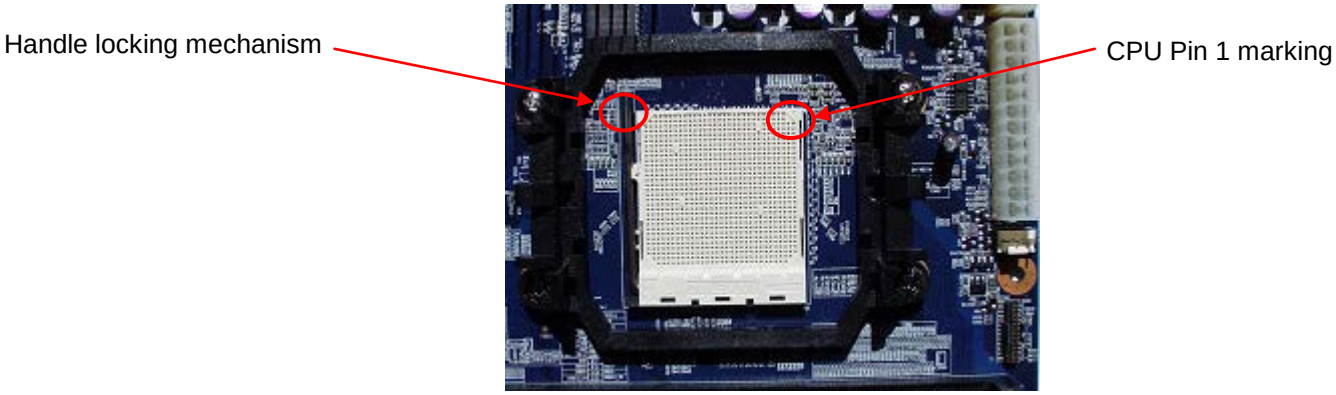
To get the board running, follow these steps. In some cases the board shipped from KONTRON Technology has CPU, DDR2 DRAM and Cooler mounted. In this case Step 2-4 can be skipped.

1. **Turn off the power supply**

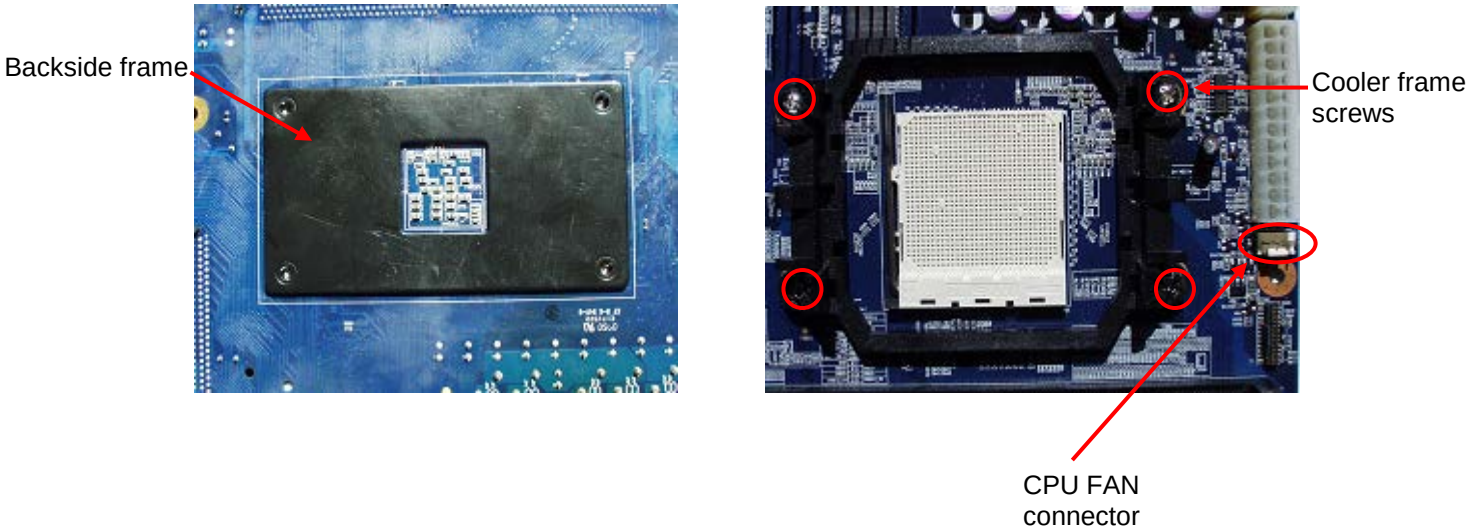
> **Warning**: Do not use Power Supply without 3.3V monitoring watchdog, which is standard feature in ATX Power Supplies.
> Running the board without 3.3V connected will damage the board after a few minutes.

2. **Insert the DDR2 DIMM 240pin DRAM module(s)**
   Push down the module from the top side until the tabs lock. For a list of approved DDR2 DIMM modules contact your Distributor or FAE.
   DDR2-667 DIMM 240pin DRAM modules (PC5300) , DDR2-800 DIMM 240pin DRAM modules (PC6400) are supported.

3. **Install the processor**
   The CPU is keyed and will only mount in the CPU socket in one way. Use the handle to open/ close the CPU socket. The AMD Phenom ™, AMD Athlon X2 64 ™, AMD Athlon X2 ™, and Sempron Processors for AM2/AM2+ socket are supported, refer to supported processor overview for details.



4. **Cooler Installation**
   A standard AM2/AM2+ CPU cooler frame is preassembled on the board, this frame is required in the combination with Kontron approved CPU Coolers. If a customer desires to used different CPU cooler, that requires a special frame the preassembled frame may be depopulated by the customer.



5. **Connecting Interfaces**
   Insert all external cables for hard disk, keyboard etc. A CRT monitor must be connected in order to change CMOS settings to flat panel support.

6. **Connect Power supply**
   Connect power supply to the board by the ATX/ BTXPWR and 4-pin ATX connectors. For board to operate connection of both the ATX/BTX and 4-pin ATX (12V) connectors are required.

7. **Turn on the power on the ATX/ BTX power supply**

8. **Power Button**
   The PWRBTN_IN must be toggled to start the Power supply; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description). A “normally open” switch can be connected via the FRONTPNL connector.
   As default, activation (~ ½ sec.) of the power button makes the system toggle between turning on or shutting down. Please notice that when the button is activated in order to start shutting down sequence, the button must be release before the sequence starts, but when the button is activated in order to boot, the boot sequence start immediately when the button is activated.

9. **BIOS Setup**
   Enter the BIOS setup by pressing the <Del> key during boot up. Refer to the “BIOS Configuration / Setup“ section of this manual for details on BIOS setup.

> **Note:** To clear all CMOS settings, including Password protection, move the Clr-CMOS jumper (with or without power) for approximately 1 minute. Alternatively turn off power and remove the battery for 1 minute, but be careful to orientate the battery correctly when reinserted.

10. **Mounting the board to chassis**

> **Warning**: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the Motherboard on a chassis it is recommended using screws with integrated washer and having diameter of ~7mm.
Note: Do not use washers with teeth, as they can damage the PCB mounting hole and may cause short circuits.

2.2 Requirement according to EN60950

Users of KT780 boards should take care when designing chassis interface connectors in order to fulfill the EN60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of peripheral devices the customer has to take care about:

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3. System specification

3.1 Component main data

The table below summarizes the features of the KT780 basic motherboard.

Form factor	KT780/ATX: (305mm by 244mm / 9.6” by 12” inches)
Processor	• Support for The AMD Phenom ™, AMD Athlon X2 64 ™, AMD Athlon X2 ™, and Sempron Processors for AM2/AM2+ socket. • 125W maximum TDP • 5.2GT/s HyperTransport™ link, 2600 MHz, 16bit/16bit • Hypertransport™ 1.0, 3.0 Tunnel (I/O Bus) speed of 1000MHz, 2600 MHz • Internal L1 cache of 128KB/256KB/512KB (Single core CPUs) / 128KB x2 (Dual core CPUs) • Internal L2 cache of 512KB/1024KB/2048KB (Single core CPUs) / 512KB x2 (Dual core CPUs) • Internal L3 cache (shared) of 2048KB for AMD Phenom ™ • Processor technology of 65nm / 90nm • DDR2 memory controller and bus interface
Memory	• Dual Channel DDR2 memory architecture • 4 pcs DDR2 DIMM 240pin DRAM sockets onboard. • Support for DDR 533/667/800MHz unbuffered memory (PC2-4200/PC2-5300/PC2-6400) • Support system memory from 256MB and up to 4GB/ 32GB* (* Memory modules for support of up to 32GB may not be available) • ECC supported
Chipset	AMD Chipset consisting of: • AMD RS780 Northbridge (graphics tunnel) • ATI SB700 Southbridge (I/O hub)
Video	• Integrated ATI Radeon™ HD3200 graphics core (RV610-based) o CRT Out connector o Dual link DVI-D connector (Digital only) **KT780/ATX w. DVI Board ONLY** o Single link HDMI w. HDCP w. Audio **KT780/ATX w. HDMI Board ONLY** • Dual independent pipe support: Mirror and Dual Independent displays supported. • Full DirectX® 10.0 support. • OpenGL 2.0 support. • Maximum resolution of 2560x1600 @ 32bpp (driver limited) for a maximum DAC speed of 400MHz. • UVD Unified Video Decoding, hardware for H.264, VC-1 and MPEG-2 decode • HW Blue Ray decoding. • HD Resolution 720p, 1080i • Sideport Video Memory of 256MB w. HDMI variant only. • Unified Memory Architecture (UMA), allowing up to 512MB dynamically allocated Video Memory (System memory is allocated when it is needed).
Audio	Audio, 7.1 and 7.2 Channel High Definition Audio Codec using the Realtek ALC888 codec • Line-out • Line-in • Surround output: SIDE, LFE, CEN, BACK and FRONT • Microphone: MIC1, MIC2 • CDROM in • SPDIF Interface Onboard speaker

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I/O Control	Winbond W83627DHG LPC Bus I/O Controller
Peripheral interfaces	• Six USB 2.0 ports on I/O area • Six USB 2.0 ports on internal pinrows • Two Serial ports (RS232) • One Parallel port, SPP/EPP/ECP • Six Serial ATA-300 IDE interfaces • PS/2 keyboard and mouse ports
LAN Support	• 2x 10/100/1000Mbits/s LAN using Marvell 88E8055 controllers • RPL/PXE netboot supported. (Only when RAID is not selected). Wake On LAN (WOL) supported (only if +5VSB has not been lost in power down mode)
BIOS	• Kontron Technology / AMI BIOS (core version ??) • Support for Advanced Configuration and Power Interface (ACPI 3.0), Plug and Play o Suspend To Ram o Suspend To Disk • Secure CMOS/ OEM Setup Defaults • “Always On” BIOS power setting • RAID Support (RAID modes 0, 1, and 10) (only when PXE netboot is not selected) (for Linux O/S limitations may apply)
Expansion Capabilities	• PCI Bus routed to PCI slots (PCI Local Bus Specification Revision 2.3) o KT780/ATX: 4 slots PCI 2.3, 32 bits, 33 MHz, 5V complying • PCI-Express bus routed to PCI Express slot(s) (PCI Express 2.0) o KT780/ATX: 1 slot PCI-Express x16 with PCI-Express x16 support • PCI-Express bus routed to PCI Express slot(s) (PCI Express 2.0) o KT780/ATX: 1 slot PCI-Express x4 with PCI-Express x4 support • SMBus routed to FEATURE, PCI slot, and PCI Express connectors • LPC Bus routed to TPM connector • DDC Bus routed to CRT,DVI connector • 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector
Hardware Monitor Subsystem	• Smart Fan control system, support Thermal® and Speed® cruise for three onboard Fan control connectors: FAN_CPU, FAN_SYS and FAN_IO. • Three thermal inputs: CPU die temperature, System temperature and External temperature. External temperature input routed to FEATURE connector. (Precision +/- 3ºC) • Voltage monitoring • Intrusion detect input • SMI violations (BIOS) on HW monitor not supported. Supported by API (Windows).
Operating Systems Support	• Windows XP, 32/64bit • Windows Vista, 32/64bit • Windows 2003, 32/64bit • WinXP Embedded (limitations may apply) • Linux: Ubuntu (limitations may apply)

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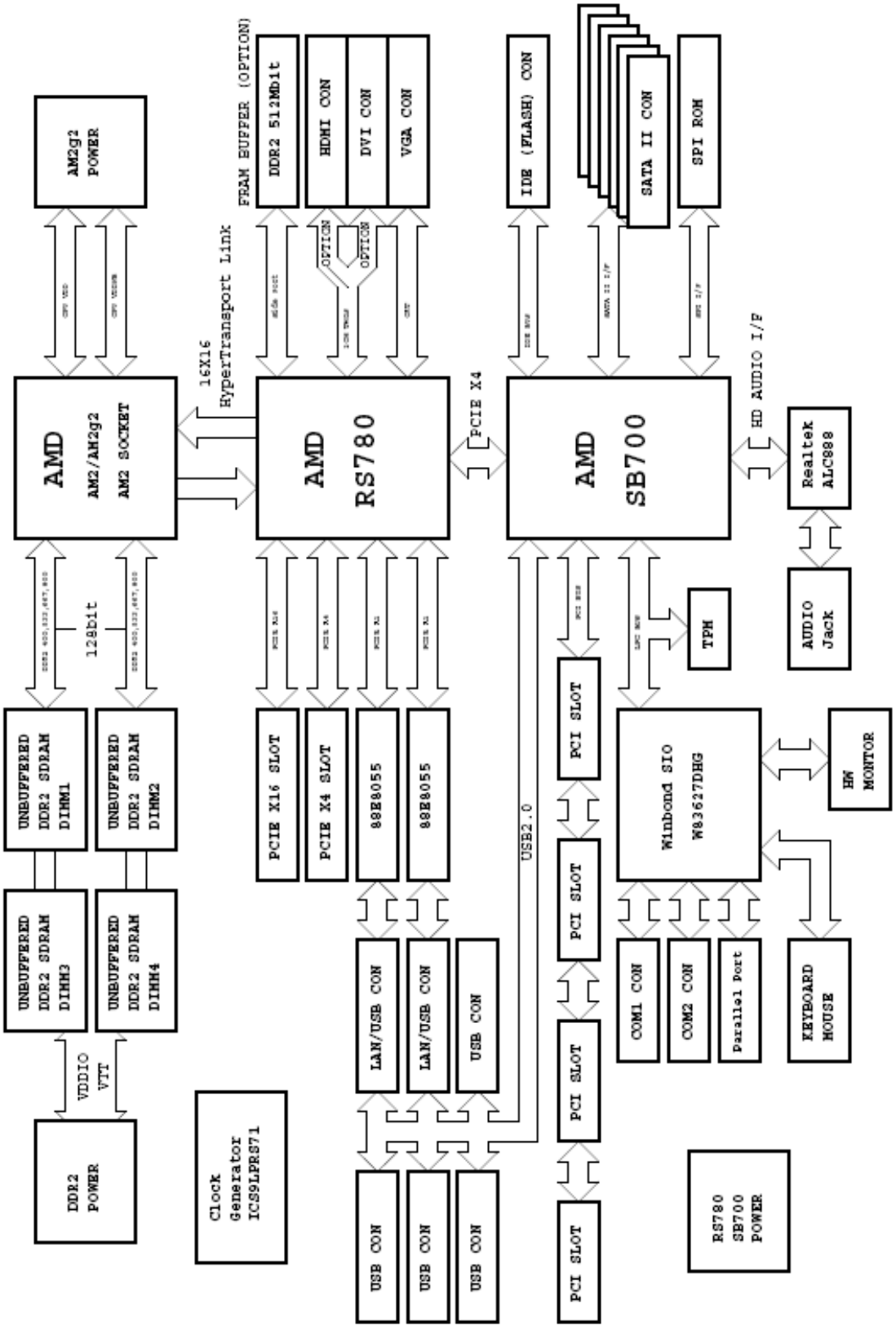
Environmental Conditions	**Operating**: 0°C – 50°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) **Storage**: -20°C – 70°C 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** UL 60950-1:2003, First Edition CSA C22.2 No. 60950-1-03 1st Ed. April 1, 2003 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Theoretical MTBF:** 305,732 hours / 34.9 years @25°C 209,338 hours / 23.9 years @40°C **Restriction of Hazardous Substances (RoHS):** All boards in the KT780 family are RoHS compliant. **Capacitor utilization:** No Tantalum capacitors on board Only Japanese brand Aluminum and solid electrolytic capacitors rated for 100° Celsius used on board
Battery	Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Panasonic / Part-number CR2032NL/LE, CR-2032L/BE or CR-2032L/BN. Approximate 5 years retention. Current draw is less that 4µA when PSU is disconnected. **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

3.2 System overview

The block diagram below shows the architecture and main components of the KT780 board. The two key components on the board are the AMD® RS780 and AMD® SB700 Embedded Chipsets.



3.3 Processor support table

The KT780 is designed to support the following socket AM2/AM2+ processors, but also support some AM3 socket processors. In the list below some examples of possible processors are listed, but many more processors up to 125W, can be used. The list is occasionally updated, but only with minor details like a few processors added. Please contact AMD for up to date information. Please notice that non embedded processors are only available for a short period of time typically 1 year while embedded processors are available for typically 5 years. In the list below the Embedded CPU's are indicated by green text, successfully tested CPU's are indicated by **highlighted** text, successfully tested embedded CPU's are indicated by **green and highlighted** text and failed CPU's are indicated by red text. Most of the embedded CPU's can be ordered at Kontron, please contact Kontron Sales Department.

AMD Processor Brand	model	Clock Speed [MHz]	Core	Order Number	Thermal Guideline [Watt]	Max. temp	Embed.
Phenom X4	9850	2500	4	HD985ZXAJ4BGH	125W	61°C	No
Phenom X4	9750	2400	4		125W		No
Phenom X4	9650	2300	4		95W		No
Phenom X4	9600	2300	4	HD9600WCJ4BGD	95W	70°C	No
Phenom X4	9550	2200	4		95W		No
Phenom X4	**9500**	**2200**	**4**	**HD9500WCJ4BGD**	**95W**	**70°C**	**No**
Phenom II XLT	**Q54L**	**2200**	**4**	**HEQ54LOEK4DGME**	**65W**	**-**	**-**
Phenom X4	9100e	1800	4		65W		No
Athlon 64 X2	**6400**	**3200**	**2**	**ADX6400IAA6CZ**	**125W**	**63°C**	**No**
Athlon II X2	**245**	**2900**	**2**	**ADX245OCK23GM**	**65W**	**74°C**	**No**
Athlon 64 X2	**5200**	**2700**	**2**	**ADO5200IAA5D0**	**65W**	**72°C**	**No**
Athlon 64 X2	4600	2400	2	ADO4600IAA5DO	65W	68°C	No
Athlon 64 X2	4200	2200	2	ADD4200IAA5DO	35W	78°C	Yes
Athlon 64 X2	**4200+**	**2200**	**2**	**ADD4200IAA5DO**	**35W**	**-**	**Yes**
Athlon II XLT	V66C	2800	2	AEV66CHDK23GME	45W	-	-
Athlon II XLT	V64L	2700	2	AEV64LHFK23GME	45W	-	-
Athlon II XLT	**V50L**	**2200**	**2**	**AEV50LSCK23GME**	**25W**	**-**	**-**
Athlon 64 X2	**3600+**	**1900**	**2**	**ADD3600IAA5DO**	**35W**	**-**	**Yes**
Athlon 64 X2	**3400e**	**1800**	**2**	**ADJ3400IAA5DOE**	**22W**	**-**	**Yes**
Athlon 64	**3100+**	**2000**	**1**	**ADS3100IAR4DRE**	**25W**	**81°C ***	**Yes**
Athlon 64	3000+	1800	1	ADD3000IAA4CNE	35W	-	Yes
Athlon 64	**2600+**	**1600**	**1**	**ADG2600IAV4DRE**	**15W**	**85°C ***	**Yes**
Athlon 64	**2000+**	**1000**	**1**	**ADF2000IAV4DRE**	**8W**	**85°C ***	**Yes**
Sempron	**LE-1300**	**2300**	**1**	**SDH1300IAA4DP**	**45W**	**75°C**	**No**
Sempron	**LE-1250**	**2200**	**1**	**SDH1250IAA4DP**	**45W**	**75°C**	**No**

*= Tcase

3.4 System Memory support

The KT780 boards have four onboard DDR2 DIMM sockets and support the following memory features:

- 1.8V (only) 240-pin DDR2 SDRAM DIMMs with gold-plated contacts
- DDR2 800 (PC6400), DDR2 667 (PC5300) or DDR2 533 MHz (PC4200) SDRAM DIMMs
- DDR2 800 DIMMs with SPD timings of only 5-5-5 or 6-6-6 (tCL-tRCD-tRP)
- Unbuffered, single-sided or double-sided DIMMs with the following restriction: Double-sided DIMMs with x16 organization are not supported.
- 32 GB maximum total system memory using 64-bit OS. (Shared Video Memory is withdrawn).
- 4 GB maximum total system memory using 32-bit OS. ~3GB is displayed in System Properties. (Shared Video Memory is withdrawn).
- Minimum total system memory: 512 MB
- ECC DIMMs supported
- Serial Presence Detect

The installed DDR2 SDRAM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted.

Important: If only one Memory module is used then use DDR2 SLOT 1.

3.4.1 Memory Operating Frequencies

Regardless of the DIMM type used, the memory frequency depends on the processor used. For example, if DDR2 800 memory is used with a processor with lower memory frequency than 800 Mhz, the memory will operate at lower frequency. The table below lists the resulting operating memory frequencies based on the combination of DIMMs and processors.

DIMM Type	Processor memory frequency	Resulting memory frequency
DDR2 533	533 MHz	533 MHz
DDR2 533	800 MHz	533 MHz
DDR2 533	1066 MHz	533 MHz
DDR2 667	533 MHz	533 MHz
DDR2 667	800 MHz	667 MHz
DDR2 667	1066 MHz	667 MHz
DDR2 800	533 MHz	533 MHz
DDR2 800	800 MHz	800 MHz
DDR2 800	1066 MHz	800 MHz

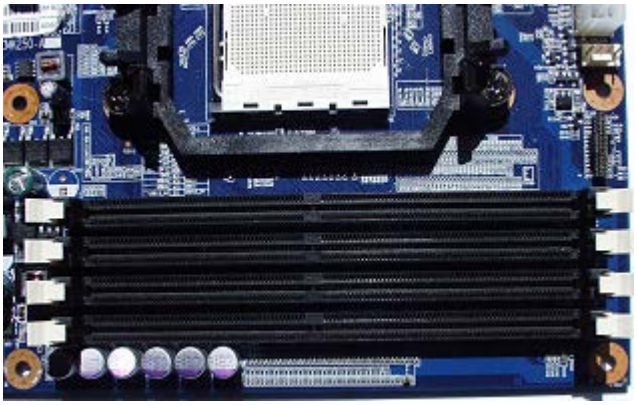
3.4.2 Memory Configurations

The KT780/ATX boards support the following three types of memory organization:

Dual channel (Interleaved) mode. This mode offers the highest throughput. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed DIMMs are used between channels, the slowest memory timing will be used.

Single channel (Asymmetric) mode. This mode is equivalent to single channel bandwidth operation. This mode is used when only a single DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speed DIMMs are used between channels, the slowest memory timing will be used.

Flex mode. This mode provides the most flexible performance characteristics. The bottommost DRAM memory (the memory that is lowest within the system memory map) is mapped to dual channel operation; the topmost DRAM memory (the memory that is nearest to the 8 GB address space limit), if any, is mapped to single channel operation. Flex mode results in multiple zones of dual and single channel operation across the whole of DRAM memory. To use flex mode, it is necessary to populate both channels.



Channel A, DDR2 DIMM 0 (SLOT 1)
Channel B, DDR2 DIMM 0 (SLOT 2)
Channel A, DDR2 DIMM 1 (SLOT 3)
Channel B, DDR2 DIMM 1 (SLOT 4)

The below tables shows examples of possible Memory slot configurations for the support of the various Memory modes.

Dual Channel (Interleaved) Mode Configurations			
Channel A		**Channel B**	
DDR2 DIMM 0 (SLOT 1)	**DDR2 DIMM 1 (SLOT 3)**	**DDR2 DIMM 0 (SLOT 2)**	**DDR2 DIMM 1 (SLOT 4)**
1 GB		1 GB	
512 MB	512 MB	1 GB	
512 MB	1 GB	512 MB	1 GB

In these examples the combined capacity of the two DIMMs in Channel A equals the combined capacity of the two DIMMs in Channel B.

Single Channel (Asymmetric) Mode Configurations			
Channel A		**Channel B**	
DDR2 DIMM 0 (SLOT 1)	**DDR2 DIMM 1 (SLOT 3)**	**DDR2 DIMM 0 (SLOT 2)**	**DDR2 DIMM 1 (SLOT 4)**
1 GB			
512 MB	1GB	1GB	

In these examples the combined capacity of the two DIMMs in Channel A does not equal the capacity of the DIMMs in Channel B.

4. Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

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The connector definitions follow the following notation:

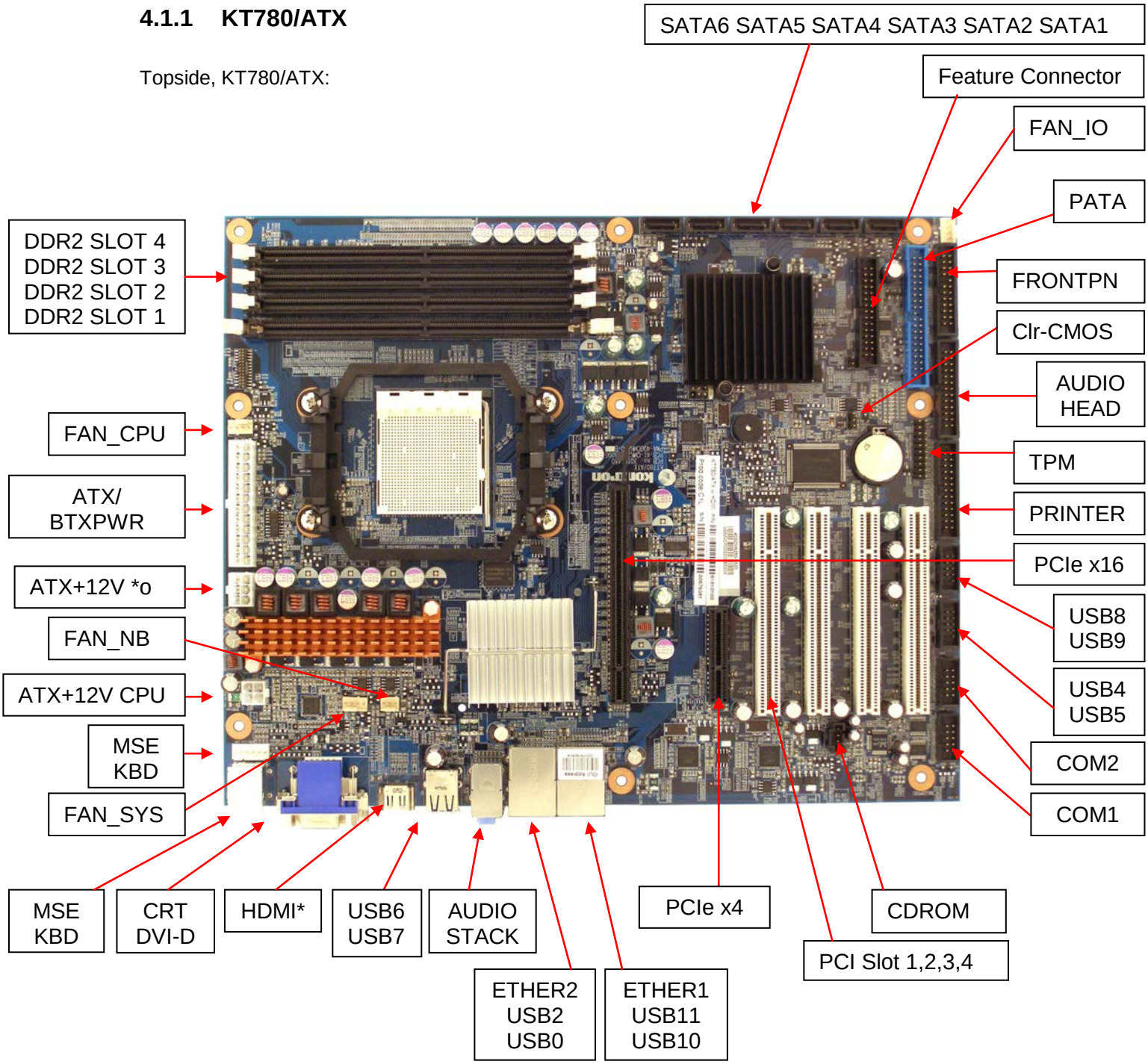
Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.
Type	AI : Analog Input. AO : Analog Output. I : Input, TTL compatible if nothing else stated. IO : Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS : Schmitt-trigger input, TTL compatible. IOC : Input / open-collector Output, TTL compatible. NC : Pin not connected. O : Output, TTL compatible. OC : Output, open-collector or open-drain, TTL compatible. OT : Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR : Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

4.1 Connector layout

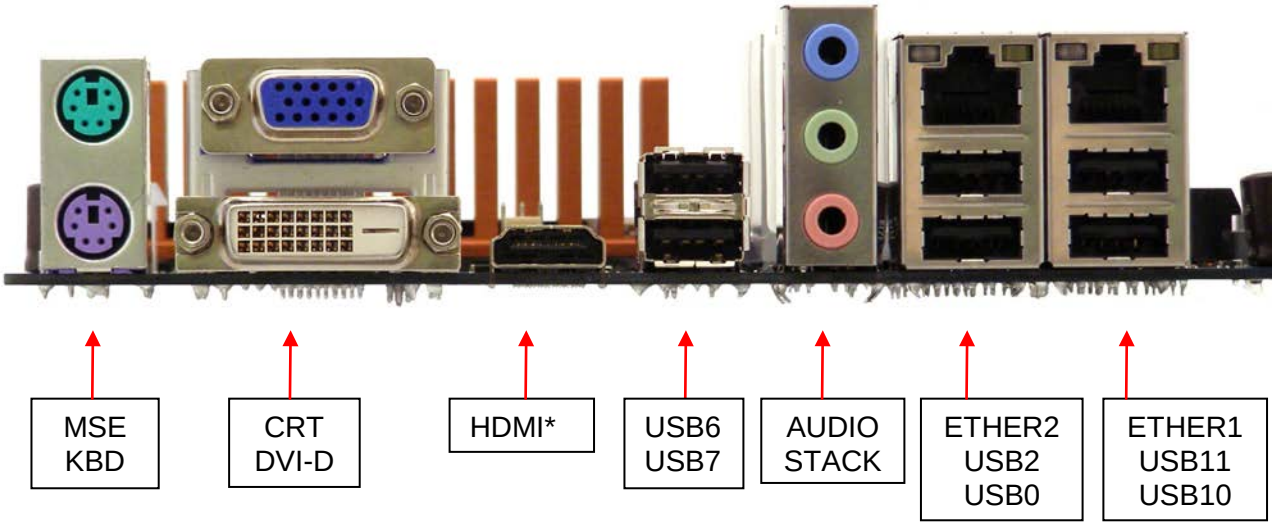
4.1.1 KT780/ATX

Topside, KT780/ATX:



* Mounted optionally.
*o Optional use.

Front, KT780/ATX



* Mounted optionally

4.2 Power Connector (ATXPWR)

The KT780 boards are designed to be supplied from a standard ATX or BTX power supply.

ATX/ BTX Power Connector:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	3V3	12	24	GND	PWR	-	-	
			PWR	+12V	11	23	5V	PWR			
			PWR	+12V	10	22	5V	PWR			
	-	-	PWR	SB5V	9	21	5V	PWR	-	-	
	-	-	I	P_OK	8	20	-5V	PWR	-	-	1
	-	-	PWR	GND	7	19	GND	PWR	-	-	
	-	-	PWR	5V	6	18	GND	PWR	-	-	
	-	-	PWR	GND	5	17	GND	PWR	-	-	
	-	-	PWR	5V	4	16	PSON#	OC	-	-	
	-	-	PWR	GND	3	15	GND	PWR	-	-	
	-	-	PWR	3V3	2	14	-12V	PWR	-	-	
	-	-	PWR	3V3	1	13	3V3	PWR	-	-	

Note 1: -5V supply is not used onboard.
Note 2: Use of BTX supply not required for operation, but may be required to drive high-power PCI Express x16 Add cards.

ATX+12V Power Connector (same net as +12V in ATX/BTX Power connector) :

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	+12V	1	4	GND	PWR	-	-	
1			PWR	+12V	2	5	GND	PWR			
			PWR	+12V	3	6	GND	PWR			

ATX+12V_CPU Power Connector:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	+12V_CPU	1	3	GND	PWR	-	-	1
1			PWR	+12V_CPU	2	4	GND	PWR			1

Note 1: Use of the 4-pin ATX+12V_CPU Power Connector is required for operation of the KT780 boards.

See chapter “Power Consumption” regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification version 2.2).

Control signal description:

Signal	Description
P_OK	P_OK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the undervoltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the undervoltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, P_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the *ATX12V Power SupplyDesign Guide*. It is strongly recommended to use an ATX or BTX supply with the KT780 boards, in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised onboard the KT780 boards.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

4.3 Keyboard and PS/2 mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signaling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resetable fuse.

4.3.1 Stacked MINI-DIN keyboard and mouse Connector (MSE & KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	-	NC	6 5	MSCLK	IOC	TBD	2K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	MSDAT	IOC	TBD	2K7	
			-	NC	6 5	KBDCLK	IOC	TBD	2K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	KBDDAT	IOC	TBD	2K7	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

4.3.2 Keyboard and mouse pin-row Connector (KBDMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	TBD	4K7	
2	KBDDAT	IOC	TBD	4K7	
3	MSCLK	IOC	TBD	4K7	
4	MSDAT	IOC	TBD	4K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

4.4 Display Connectors

The KT780 board provides:

1. Analog CRT interface (Front panel)
2. Digital DVI (DVI-D) (Front panel)
3. HDMI connector (Front panel)

The KT780 board does not support ADD2 / SDVO cards on the PCI Express x16 connector.

The KT780 integrates the ATI Radeon™ HD3200 Graphics Core with support for Dual Clone display and Dual independent display.

The supported combinations are listed in the below matrix:

		Primary Display		
		CRT	**DVI-D**	**HDMI**
Secondary Display	**CRT**		Clone / Dual	Clone / Dual
	DVI-D	Clone / Dual		
	HDMI	Clone / Dual		

TBD: To be determined.

4.4.1 CRT Connector (CRT)

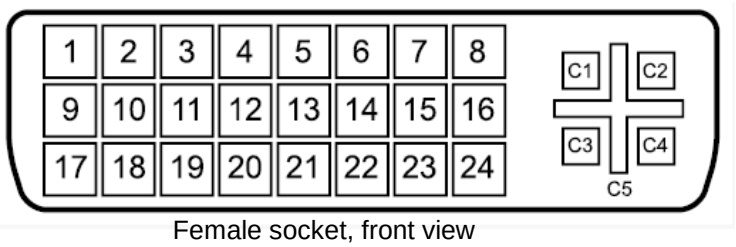
Note	Pull U/D	Ioh/Iol	Type	Signal	PIN			Signal	Type	Ioh/Iol	Pull U/D	Note
						6		GND	PWR	-	-	
	/75R	*	A0	RED	1		11	NC	-	-	-	
						7		GND	PWR	-	-	
	/75R	*	A0	GREEN	2		12	DDCDAT	IO	TBD	6K81	2
						8		GND	PWR	-	-	
	/75R	*	A0	BLUE	3		13	HSYNC	O	TBD		
						9		5V	PWR	-	-	1
	-	-	-	NC	4		14	VSYNC	O	TBD		
						10		GND	PWR	-	-	
	-	-	PWR	GND	5		15	DDCCLK	IO	TBD	6K81	2

Note 1: The 5V supply in the CRT connector is fused by a 1.1A reset-able fuse.
Note 2: Pull-up to +5V.

Signal Description - CRT Connector:

Signal	Description
HSYNC	CRT horizontal synchronization output.
VSYNC	CRT vertical synchronization output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red color signal to the CRT. For 75 Ohm cable impedance.
GREEN	Analog output carrying the green color signal to the CRT. For 75 Ohm cable impedance.
BLUE	Analog output carrying the blue color signal to the CRT. For 75 Ohm cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

4.4.2 DVI Connector (DVI-D, digital only) Dual Link



Female socket, front view

Note 1: Pins C1-C5 (DVI analogue signals) are not supported, but may be present for compatibility.

Signal Description - DVI Connector:

Pin No.	Signal	Description	Type	Pull Up
1	TMDS Data 2-	(Link 1)	LVDS	
2	TMDS Data 2+	(Link 1)	LVDS	
3	TMDS Data 2/4 Shield		PWR	
4	TMDS Data 1-	(Link 2)	LVDS	
5	TMDS Data 1+	(Link 2)	LVDS	
6	DDC Clock	DDC Clock	IO	6K8
7	DDC Data	DDC Data	IO	6K8
8	N.C.		-	
9	TMDS Data 1-	(Link 1)	LVDS	
10	TMDS Data 1+	(Link 1)	LVDS	
11	TMDS Data 1/3 Shield		PWR	
12	TMDS Data 0-	(Link 2)	LVDS	
13	TMDS Data 0+	(Link 2)	LVDS	
14	+5V		PWR	
15	GND		PWR	
16	Hot Plug Detect	Hot Plug Detect	I	
17	TMDS Data 0-	(Link 1)	LVDS	
18	TMDS Data 0+	(Link 1)	LVDS	
19	TMDS Data 0/5 Shield		PWR	
20	TMDS Data 2-	(Link 2)	LVDS	
21	TMDS Data 2+	(Link 2)	LVDS	
22	TMDS Clock Shield		PWR	
23	TMDS Clock+	Digital clock + (Link 1)	LVDS	
24	TMDS Clock-	Digital clock - (Link 1)	LVDS	
C1 - C5	N.C.		-	

4.4.3 High Definition Multimedia Interface HDMI Connector Single link.

Signal Description – HDMI Flat Panel Connector:

Pin No.	Signal	Description	Type	Pull Up
1	TMDS Data 2+		LVDS	
2	TMDS Data 1/3 Shield		PWR	
3	TMDS Data 2-		LVDS	
4	TMDS Data 1+		LVDS	
5	TMDS Data 4/6 Shield		PWR	
6	TMDS Data 1-		LVDS	
7	TMDS Data 0+		LVDS	
8	TMDS Data 7/9 Shield		PWR	
9	TMDS Data 0-		LVDS	
10	TMDS Clock+		LVDS	
11	TMDS Clock Shield		PWR	
12	TMDS Clock-		LVDS	
13	N.C.		-	
14	N.C.		-	
15	DDC Clock (N.C.)	DDC Clock	IO	6K8
16	DDC Data (N.C.)	DDC Data	IO	6K8
17	GND		PWR	
18	+5V		PWR	
19	Hot Plug Detect	Hot Plug Detect	I	
20	GND		PWR	

4.5 PCI-Express x16 Connectors

The KT780 board contains one 16-lane (x16) PCI Express port on a PCI Express x16 connector. The PCI Express port is compliant to the PCI Express Specification revision 2.0.

The x16 port operates at a frequency of 5.0 Gb/s on each lane; the port supports a maximum theoretical bandwidth of 16 Gbyte/s in each direction.

The 16-lane (x16) PCI Express rev2 port supports:

1. An external graphics device utilizing all 16 lanes
2. Supports x4, x8 or x16 graphics devices

The PCI Express port does not support SDVO and ADD2 cards.

4.5.1 PCI-Express x16

The KT780 boards supports one 16-lane (x16) PCI Express port for external PCI Express based graphics boards.

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	COMM_EN		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	DP_AUX1_P		
		GND	B7	A7	DP_AUX1_N		
		+3V3	B8	A8	NC		
		TMDS_HPD1	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLK		
		GFX_TXP[0]	B14	A14	PCIE_x16 CLK#		
		GFX_TXN[0]	B15	A15	GND		
		GND	B16	A16	GFX_RXP[0]		
		SC_AUX0_P	B17	A17	GFX_RXN[0]		
		GND	B18	A18	GND		
		GFX_TXP[1]	B19	A19	NC		
		GFX_TXN[1]	B20	A20	GND		
		GND	B21	A21	GFX_RXP[1]		
		GND	B22	A22	GFX_RXN[1]		
		GFX_TXP[2]	B23	A23	GND		
		GFX_TXN[2]	B24	A24	GND		
		GND	B25	A25	GFX_RXP[2]		
		GND	B26	A26	GFX_RXN[2]		
		GFX_TXP[3]	B27	A27	GND		
		GFX_TXN[3]	B28	A28	GND		
		GND	B29	A29	GFX_RXP[3]		
		NC	B30	A30	GFX_RXN[3]		
		SD_AUX0_N	B31	A31	GND		
		GND	B32	A32	NC		
		GFX_TXP[4]	B33	A33	NC		
		GFX_TXN[4]	B34	A34	GND		
		GND	B35	A35	GFX_RXP[4]		
		GND	B36	A36	GFX_RXN[4]		
		GFX_TXP[5]	B37	A37	GND		
		GFX_TXN[5]	B38	A38	GND		
		GND	B39	A39	GFX_RXP[5]		
		GND	B40	A40	GFX_RXN[5]		
		GFX_TXP[6]	B41	A41	GND		
		GFX_TXN[6]	B42	A42	GND		
		GND	B43	A43	GFX_RXP[6]		
		GND	B44	A44	GFX_RXN[6]		
		GFX_TXP[7]	B45	A45	GND		
		GFX_TXN[7]	B46	A46	GND		
		GND	B47	A47	GFX_RXP[7]		

(continues)

		TMDS_HPD0	B48	A48	GFX_RXN[7]		
		GND	B49	A49	GND		
		GFX_TXP[8]	B50	A50	NC		
		GFX_TXN[8]	B51	A51	GND		
		GND	B52	A52	GFX_RXP[8]		
		GND	B53	A53	GFX_RXN[8]		
		GFX_TXP[9]	B54	A54	GND		
		GFX_TXN[9]	B55	A55	GND		
		GND	B56	A56	GFX_RXP[9]		
		GND	B57	A57	GFX_RXN[9]		
		GFX_TXP[10]	B58	A58	GND		
		GFX_TXN[10]	B59	A59	GND		
		GND	B60	A60	GFX_RXP[10]		
		GND	B61	A61	GFX_RXN[10]		
		GFX_TXP[11]	B62	A62	GND		
		GFX_TXN[11]	B63	A63	GND		
		GND	B64	A64	GFX_RXP[11]		
		GND	B65	A65	GFX_RXN[11]		
		GFX_TXP[12]	B66	A66	GND		
		GFX_TXN[12]	B67	A67	GND		
		GND	B68	A68	GFX_RXP[12]		
		GND	B69	A69	GFX_RXN[12]		
		GFX_TXP[13]	B70	A70	GND		
		GFX_TXN[13]	B71	A71	GND		
		GND	B72	A72	GFX_RXP[13]		
		GND	B73	A73	GFX_RXN[13]		
		GFX_TXP[14]	B74	A74	GND		
		GFX_TXN[14]	B75	A75	GND		
		GND	B76	A76	GFX_RXP[14]		
		GND	B77	A77	GFX_RXN[14]		
		GFX_TXP[15]	B78	A78	GND		
		GFX_TXN[15]	B79	A79	GND		
		GND	B80	A80	GFX_RXP[15]		
		NC	B81	A81	GFX_RXN[15]		
		NC	B82	A82	GND		

4.6 PCI-Express x4 Connectors

The KT780 board contains one 4-lane (x4) PCI Express port on a PCI Express x4 connector. The PCI Express port is compliant to the PCI Express Specification revision 2.0.

The x4 port operates at a frequency of 5.0 Gb/s on each lane; the port supports a maximum theoretical bandwidth of 4 Gbyte/s in each direction.

The 4-lane (x4) PCI Express rev2 port supports:

1. An external general purpose device utilizing all 4 lanes
2. Supports x1, x2 or x4 general purpose devices

4.6.1 PCI-Express x4

The KT780 boards supports one 4-lane (x4) PCI Express port for external PCI Express general purpose boards.

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	GPP_CLK1P		
		GPP_TXP[0]	B14	A14	GPP_CLK1N		
		GPP _TXN[0]	B15	A15	GND		
		GND	B16	A16	GPP_RXP[0]		
		NC	B17	A17	GPP_RXN[0]		
		GND	B18	A18	GND		
		GPP_TXP[1]	B19	A19	NC		
		GPP_TXN[1]	B20	A20	GND		
		GND	B21	A21	GPP_RXP[1]		
		GND	B22	A22	GPP_RXN[1]		
		GPP_TXP[2]	B23	A23	GND		
		GPP_TXN[2]	B24	A24	GND		
		GND	B25	A25	GPP_RXP[2]		
		GND	B26	A26	GPP_RXN[2]		
		GPP_TXP[3]	B27	A27	GND		
		GPP_TXN[3]	B28	A28	GND		
		GND	B29	A29	GPP_RXP[3]		
		NC	B30	A30	GPP_RXN[3]		
		NC	B31	A31	GND		
		GND	B32	A32	NC		

4.7 Parallel ATA harddisk interface

One parallel ATA harddisk controllers is available on the board – a primary controller. Standard 3½" harddisks or CD-ROM drives may be attached to the primary controller by means of the 40 pin IDC connector, PATA.

The parallel ATA harddisk controller is shared between the PATA connector and the Hyperflash adapter (Accessory). Hyperflash adapter and PATA disk are not supported at the same time.

The harddisk controllers support Bus master IDE, ultra DMA 33/66/100/133 MHz and standard operation modes. For support of ultra DMA 66/100/133 MHz, a 80 wire cable is required.

The signals used for the harddisk interface are the following:

Signal	Description
DAA2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCSA1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
DA15..8	High part of data bus.
DA7..0	Low part of data bus.
IORA#	I/O Read.
IOWA#	I/O Write.
IORDYA#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESETA#	Reset signal to the hard disk.
HDIRQA	Interrupt line from hard disk.
CBLIDA	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQA	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACKA#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACTA#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

All of the above signals are compliant to [4].
The pinout of the connectors are defined in the following sections.

4.7.1 IDE Hard Disk Connector (PATA)

This connector can be used for connection of two primary IDE drives.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESET_P#	1	2	GND	PWR	-	-	
	-	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	O	IOWA#	23	24	GND	PWR	-	-	
	-	TBD	O	IORA#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYA	27	28	GND	PWR	-	-	
	-	-	O	DDACKA#	29	30	GND	PWR	-	-	
	10K	-	I	HDIRQA	31	32	NC	-	-	-	
	-	TBD	O	DAA1	33	34	CBLIDA#	I	-		
	-	TBD	O	DAA0	35	36	DAA2	O	TBD	-	
	-	TBD	O	HDCSA0#	37	38	HDCSA1#	O	TBD	-	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

4.8 Serial ATA harddisk interface

The KT780 boards have an integrated SATA Host controller that supports independent operation on six ports and data transfer rates of up to 3.0Gb/s (300MB/s). The SATA controller supports AHCI mode and has integrated RAID functionality with support for RAID modes 0, 1 and 10.

The board provides four Serial ATA (SATA) connectors, which support one device per connector.
The S700 Southbridge Serial ATA controller offers four independent Serial ATA ports with a theoretical maximum transfer rate of 3 Gbits/sec per port.
A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.
For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). Legacy mode is only supported on four SATA port(s). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows XP and Windows Vista operating systems.

The KT780 supports the following RAID (Redundant Array of Independent Drives) levels:
- RAID 0 - data striping
- RAID 1 - data mirroring
- RAID 0+1 (or RAID 10) - data striping and mirroring

Limitations depending on Target Operating System apply.

Note: The PCB silkscreen of SATA connectors, are not related to how the BIOS list detected devices.

4.8.1 SATA Hard Disk Connector (SATA1, SATA2, SATA3, SATA4, SATA5, SATA6)

SATA:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA* TX+				
3	SATA* TX-				
4	GND	PWR	-	-	
5	SATA* RX-				
6	SATA* RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA harddisk interface are the following:

Signal	Description
SATA* RX+ SATA* RX-	Host transmitter differential signal pair
SATA* TX+ SATA* TX-	Host receiver differential signal pair

"*" specifies 1, 2, 3, 4, 5 and 6 depending on SATA port.
All of the above signals are compliant to [6].

Note: BIOS setting "SATA IDE Combined Mode" must be Enabled for using SATA port 5 & 6.

4.9 Printer Port Connector (PRINTER).

The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1	2	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	3	4	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	5	6	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	7	8	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	9	10	GND	PWR	-	-	
	2K2	24/24	IO	PD4	11	12	GND	PWR	-	-	
	2K2	24/24	IO	PD5	13	14	GND	PWR	-	-	
	2K2	24/24	IO	PD6	15	16	GND	PWR	-	-	
	2K2	24/24	IO	PD7	17	18	GND	PWR	-	-	
	2K2	-	I	ACK#	19	20	GND	PWR	-	-	
	2K2	-	I	BUSY	21	22	GND	PWR	-	-	
	2K2	-	I	PE	23	24	GND	PWR	-	-	
	2K2	-	I	SLCT	25	26	GND	PWR	-	-	

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

Signal	Description
PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode as defined in [3].

4.10 Serial Ports

Two RS232 serial ports are available on the KT780/ATX board

The typical interpretation of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitte Data, sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Receive Data, receives serial data from the communication link.
DTR	Data Terminal Ready, indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send, indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

4.10.1 Com1 Pin Header Connector.

The pinout of Serial ports Com1 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: The Com1 header 5V supply is not fused.

A DB9 adapter (ribbon cable) can be used to make a DB9 pinout available.

4.10.2 Com2 Pin Header Connector.

The pinout of Serial ports Com2 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: The Com2 header 5V supply is not fused.

A DB9 adapter (ribbon cable) can be used to make a DB9 pinout available.

4.11 Ethernet connectors.

The KT780/ATX boards supports 2 channels of 10/100/1000Mb Ethernet Marvell 88E8055 LAN controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[0]-	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]-	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair.
MDI[2]-	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.
MDI[3]-	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

4.11.1 Ethernet connectors (ETHER1 and ETHER2)

Ethernet connector 1 is mounted together with USB Ports 10 and 11.
Ethernet connector 2 is mounted together with USB Ports 0 and 2.

The pinout of the RJ45 connector is as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2+				
MDI2-				
MDI1-				
MDI3+				
MDI3-				
	8 7 6 5 4 3 2 1			

4.12 USB Connector (USB)

The KT780 boards contains two Enhanced Host Controller Interface (EHCI) host controllers that supports USB 2.0 allowing data transfers up to 480Mb/s. The KT780 boards also contains four Open Host Controller Interface (OHCI) controllers that support USB full-speed and low-speed signaling (USB 1.1).

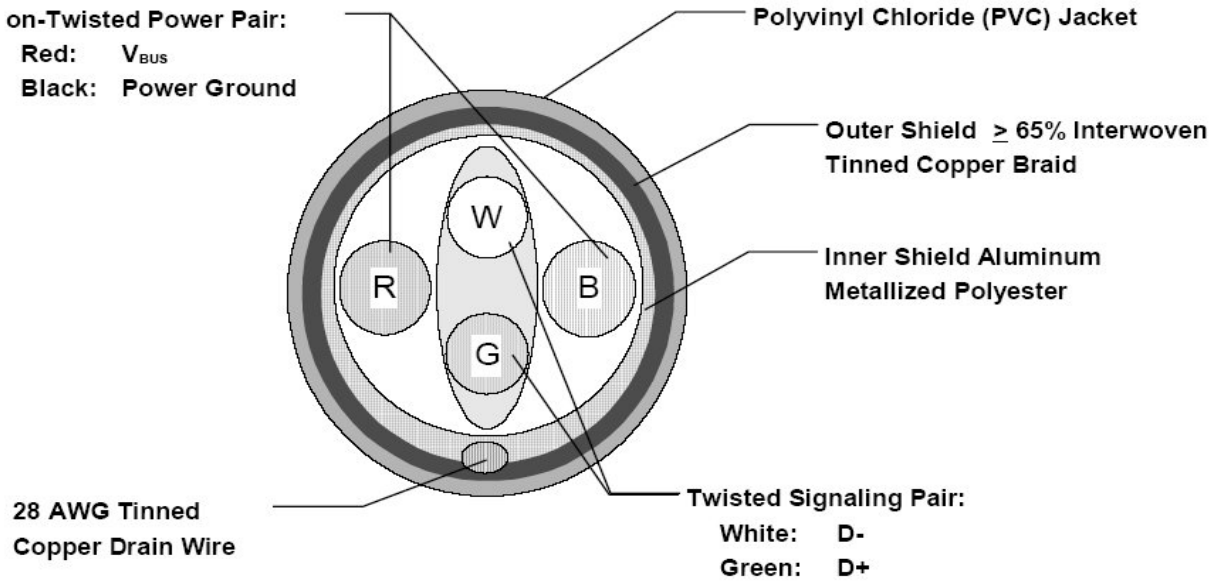
The KT780 boards supports a total of twelve USB 2.0 ports. All twelve ports are high-speed (USB 2.0), full-speed (USB 1.1), and low-speed (USB 1.1) capable and USB Legacy mode is supported.

On all USB ports SB5V is supplied during power down to allow wakeup on USB device activity. Note that in order to wakeup on USB activity a Windows XP registry file setting is required and SB5V must be applied always (no loss) during power down.

Over-current detection on all ten USB ports is supported.

USB Port 0 and 2 are supplied on the combined ETHER2 USB0, USB2 connector.
USB Ports 1 and 3 are supplied on the internal FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.
USB Port 4 and 5 are supplied on the internal USB4, USB5 pinrow connector.
USB Port 6 and 7 are supplied on the USB6, USB7 frontpanel connector.
USB Port 8 and 9 are supplied on the internal USB8, USB9 pinrow connector.
USB Port 10 and 11 are supplied on the combined ETHER1 USB10, USB11 connector.

Note: It is recommended to use only High-/Full-Speed USB cable, specified in USB2.0 standard:



4.12.1 USB Connector 0/2 (USB0/2)

USB Port 0 and 2 are supplied on the combined ETHER2 USB0, USB2 connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB2-		USB2+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB0-		USB0+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB2+ USB2- USB0+ USB0-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.12.2 USB Connector 1/3 (USB1/3)

USB Ports 1 and 3 are supplied on the internal FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-		1
		-	IO	USB1-	3	4	USB3-	IO		-	
	-		IO	USB1+	5	6	USB3+	IO	-		
	-		PWR	GND	7	8	GND	PWR	-		
	-	-		KEY	9	10	LINE2-L		-	-	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB1+ USB1- USB3+ USB3-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.12.3 USB Connector 4/5 (USB4/5)

USB Port 4 and 5 are supplied on the internal USB4, USB5 pinrow connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-		1
		-	IO	USB4-	3	4	USB5-	IO		-	
	-		IO	USB4+	5	6	USB5+	IO	-		
	-		PWR	GND	7	8	GND	PWR	-		
	-	-		KEY	9	10	NC		-	-	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB4+ USB4- USB5+ USB5-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.12.4 USB Connector 6/7 (USB6/7)

USB Port 6 and 7 are supplied on the USB6, USB7 frontpanel connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB6-		USB6+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB7-		USB7+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB6+ USB6- USB7+ USB7-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.12.5 USB Connector 8/9 (USB8/9)

USB Port 8 and 9 are supplied on the internal USB8, USB9 pinrow connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-		1
		-	IO	USB8-	3	4	USB9-	IO		-	
	-		IO	USB8+	5	6	USB9+	IO	-		
	-		PWR	GND	7	8	GND	PWR	-		
	-	-		KEY	9	10	NC		-	-	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB8+ USB8- USB9+ USB9-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.12.6 USB Connector 10/11 (USB10/11)

USB Port 10 and 11 are supplied on the combined ETHER1 USB10, USB11 connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB11-		USB11+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB10-		USB10+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB11+ USB11- USB10+ USB10-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.13 Audio Connector

The onboard Audio circuit implements 7.1+2 Channel High Definition Audio, featuring ten 24-bit stereo DACs and two 20-bit stereo ADCs.
The Audio signals are made available on the Frontpanel stacked connector (Line in / Line out / MIC) and the onboard AUDIO_HEAD and CDROM Audio input connectors.

4.13.1 Audio Line-in, Line-out and Microphone

Audio Line-in, Line-out and Microphone are available in the stacked audio jack connector.

IN	Signal	Type	Note
TIP	LINE1-IN-L	IA	1
RING	LINE1-IN-R	IA	1
SLEEVE	GND	PWR	
TIP	FRONT-OUT-L	OA	
RING	FRONT-OUT-R	OA	
SLEEVE	GND	PWR	
TIP	MIC1-L	IA	1
RING	MIC1-R	IA	1
SLEEVE	GND	PWR	

Note 1: Signals are shorted to GND internally in the connector, when jack-plug not inserted.

4.13.2 CD-ROM Audio input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	1

Note 1: The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is **not** shorted to the general digital GND on the board).

Note: To make the CD-ROM Audio input play, open Realtek audio software-Mixer, select Tool (in left corner) and select "Advanced playback of multi streaming".

4.13.3 AUDIO Header (AUDIO_HEAD)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
				LFE-OUT	1	2	CEN-OUT				
				AAGND	3	4	AAGND				
				FRONT-OUT-L	5	6	FRONT-OUT-R				
				AAGND	7	8	AAGND				
				REAR-OUT-L	9	10	REAR-OUT-R				
				SIDE-OUT-L	11	12	SIDE-OUT-R				
				AAGND	13	14	AAGND				
				MIC1-L	15	16	MIC1-R				
				AAGND	17	18	AAGND				
				LINE1-IN-L	19	20	LINE1-IN-R				
				NC	21	22	AAGND				
	-	-	PWR	GND	23	24	SPDIF-IN				
				SPDIF-OUT	25	26	GND	PWR	-	-	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
NC	No connection	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	
F-SPDIF-IN	S/PDIF Input	
F-SPDIF-OUT	S/PDIF Output	
AAGND	Audio Analogue ground	

4.14 Fan connectors , FAN_CPU, FAN_SYS, FAN_IO and FAN_NB.

The **FAN_CPU** is used for connection of the active cooler for the CPU.
The **FAN_SYS** can be used to power, control and monitor a fan for chassis ventilation etc.
The **FAN_IO** can be used to power, control and monitor a fan for chassis ventilation etc.
The **FAN_NB** is used for connection of the active cooler for the North bridge (Optional, 3-pin only).

The 4pin header supports connection of 3-pin FANs, but it is recommended to use the 4-pin type for optimized FAN speed control. The 3- or 4-pin mode is controlled in the BIOS setup menu.

4-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CONTROL	O	-	-	
2	SENSE	I	-	4K7 to 12V	
3	+12 V	PWR	-	-	
4	GND	PWR	-	-	

Signal	Description
CONTROL	PWM signal for FAN speed control
SENSE	Tacho signal input with on board pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.
12V	+12V supply for fan. A maximum of 2000 mA can be supplied from this pin.
GND	Power Supply GND signal

3-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
2	SENSE	I	-	4K7 to 12V	
3	+12 V	PWR	-	-	
4	GND	PWR	-	-	

Signal	Description
SENSE	Tacho signal input with on board pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 2000 mA can be supplied from this pin.
GND	Power Supply GND signal

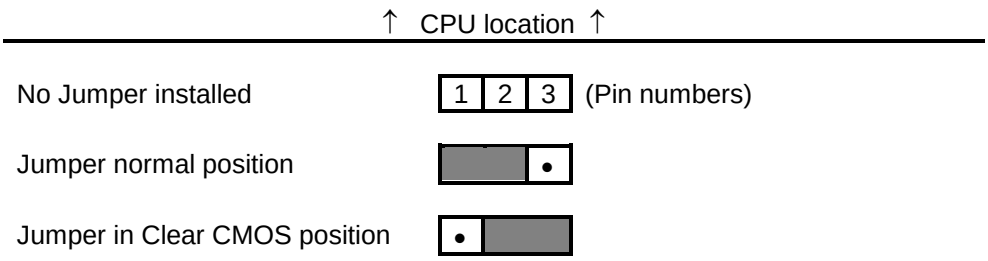
3-pin Native for North bridge:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	SENSE	I	-	4K7 to 12V	
2	+12 V	PWR	-	-	
3	GND	PWR	-	-	

Signal	Description
SENSE	Tacho signal input with on board pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 2000 mA can be supplied from this pin.
GND	Power Supply GND signal

4.15 The Clear CMOS Jumper, Clr-CMOS.

The Clr-CMOS Jumper is used to clear the CMOS content.



To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power on the system) for approximately 1 minute.

Alternatively if no jumper is available, turn off power and remove the battery for 1 minute, but be careful to orientate the battery correctly when reinserted.

4.16 TPM connector.

Note: The KT780 board have integrated TPM device.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	LPC IRQ#				

4.17 Front Panel connector (FRONTPNL).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
				USB13_5V	1	2	USB13_5V				
				USB1-	3	4	USB3-				
				USB1+	5	6	USB3+				
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	-	KEY		10	LINE2-IN-L	-	-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
			OC	HD_LED	13	14	SUS_LED				
	-	-	PWR	GND	15	16	PWRBTN_IN#				
				RSTIN#	17	18	GND	PWR	-	-	
				SB3V3	19	20	LINE2-IN-R	-	-	-	
				AGND	21	22	AGND				
1				MIC2-L	23	24	MIC2-R				1

Note 1: Unsupported inputs, leave these inputs unconnected.

Signal	Description
USB13_5V	+5V supply for the USB devices on USB Port 1 and 3 is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB3+ USB3-	Universal Serial Bus Port 3 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connector flatcable or crimp terminals respectively.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for minimum 16mS the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
LINE2-IN	Line in 2 signals
MIC2	MIC2-L and MIC2-R are unsupported. Leave these terminals unconnected.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

4.18 Feature Connector (FEATURE)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	2M/	-	I	INTRUDER#	1	2	GND	PWR	-	-	
				EXT_ISAIRQ#	3	4	EXT_SMI#	I			
				PWR_OK	5	6	SB5V	PWR	-	-	
	-	-	PWR	SB3V3	7	8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9	10	GND	PWR	-	-	
1	4K7/	/12mA	IOT	GPIO0	11	12	GPIO1	IOT	/12mA	2K7/	1
1	4K7/	/12mA	IOT	GPIO2	13	14	GPIO3	IOT	/12mA	2K7/	1
1	4K7/	/12mA	IOT	GPIO4	15	16	GPIO5	IOT	/12mA	2K7/	3
3	4K7/	/12mA	IOT	GPIO6	17	18	GPIO7	IOT	/12mA	2K7/	3
	-	-	PWR	GND	19	20	FAN3OUT				
				FAN3IN	21	22	+12V	PWR	-	-	
				TEMP3IN	23	24	VREF				
	-	-	PWR	GND	25	26	IRRX				
				IRTX	27	28	GND	PWR	-	-	
1	2K7/			SMBC	29	30	SMBD			2K7/	1

Note 1: Pull-up to +3V3Dual (+3V3 or SB3V3). Note 2: Pull-up to RTC-Voltage. Note 3: Pull-up to +3V3.

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not needed.
EXT_ISAIRQ#	EXTernal ISA IRQ, (active low input) can activate standard AT-Bus IRQ-interrupt.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures is detected.
SB5V	StandBy +5V supply.
SB3V3	Max. load is 0.75A (1.5A < 1 sec.)
EXT_BAT	(EXTernal BATtery) the + terminal of an external primary cell battery can be connected to this pin. The – terminal of the battery shall be connected to GND (etc. pin 10). The external battery is protected against charging and can be used with or without the on board battery installed. The external battery voltage shall be in the range: 2.5 - 4.0 V DC. Current draw is 3µA when PSU is disconnected.
+5V	Max. load is 0.75A (1.5A < 1 sec.)
GPIO0..7	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KONTRON API (Application Programming Interface) available for WinXP and Windows Vista.
FAN3OUT	FAN 3 speed control OUTput. This analogue voltage output signal can be set to output voltages from 0 – 3V3 to control the Fan's speed.. For more information please look into the datasheet for the Winbond I/O controller W83627.
FAN3IN	FAN3 Input. 0V to +3V3 amplitude Fan 3 tachometer input.
+12V	Max. load is 0.75A (1.5A < 1 sec.)
TEMP3IN	Temperature sensor 3 input. (Recommended: Transistor 2N3904, having emitter connected to GND (pin 25), collector and basis shorted and connected to pin23 (Temp3-In). Further a resistor 30K/1% shall be connected between pin 23 and pin 24 (Vref). (Precision +/- 3ºC)
VREF	Voltage REFerence, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal

4.19 PCI Slot Connector

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
		NC	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
		NC	F09	E09	NC		
		NC	F10	E10	+5V (I/O)	PWR	
		NC	F11	E11	NC	O	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
		NC	F14	E14	3V3	OT	
	PWR	GND	F15	E15	RST#	O	
	O	PCICLK	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	PME#	O	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	IDSEL	IOT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SMB_CLK	IO	
	PWR	+3.3V	F41	E41	SMB_DATA	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE					**COMPONENT SIDE**		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
8K2/ PU	IOT	ACK64#	F60	E60	REQ64#	IOT	8K2/ PU
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

4.19.1 Signal Description –PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

(continues)

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted.
	While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the □signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

5. System Resources

5.1 Memory map

Address range (hex)		Size (bytes)	Description
00000000	0009FFFF	655360	System board
000A0000	000BFFFF	131072	ATI Radeon HD 3200 Graphics
000A0000	000BFFFF	131072	PCI standard PCI to PCI-Bridge
000A0000	000BFFFF	131072	PCI-bus
000C0000	000CFFFF	65536	System board
000D0000	000DFFFF	65536	PCI-bus
000E0000	000FFFFF	131072	System board
00100000	6FFFFFFF	1877999616	System board (2 GB Memory – VGA Memory)
70000000	7FFFFFFF	268435456	Motherboard resources
70000000	DFFFFFFF	1879048192	PCI-bus
D0000000	DFFFFFFF	268435456	ATI Radeon HD 3200 Graphics
D0000000	DFFFFFFF	268435456	PCI standard PCI to PCI-Bridge
E0000000	EFFFFFFF	268435456	Motherboard resources
F0000000	FEBFFFFF	247463936	PCI-bus
FE7CC000	FE7CFFFF	16384	Microsoft UAA Bus Driver for High Definition Audio
FE7DA000	FE7DAFFF	4096	Standard OpenHCD USB Host Controller
FE7DB000	FE7DBFFF	4096	Standard OpenHCD USB Host Controller
FE7F0000	FE7F0FFF	4096	Standard OpenHCD USB Host Controller
FE7F1000	FE7F1FFF	4096	Standard OpenHCD USB Host Controller
FE7F2000	FE7F2FFF	4096	Standard OpenHCD USB Host Controller
FE7F3400	FE7F34FF	256	Standard Enhanced PCI to USB Host Controller
FE7F3800	FE7F38FF	256	Standard Enhanced PCI to USB Host Controller
FE7F3C00	FE7F3FFF	1024	Standard Dual Channel PCI IDE-controller
FE800000	FE8FFFFF	1048576	ATI Radeon HD 3200 Graphics
FE800000	FE9FFFFF	2097152	PCI standard PCI to PCI-Bridge
FE9E8000	FE9EBFFF	16384	Microsoft UAA Bus Driver for High Definition Audio
FE9F0000	FE9FFFFF	65536	ATI Radeon HD 3200 Graphics
FEA00000	FEAFFFFF	1048576	PCI standard PCI to PCI-Bridge
FEAFC000	FEAFFFFF	16384	Marvell Yukon 88E8055 PCI-E Gigabit Ethernet
FEB00000	FEBFFFFF	1048576	PCI standard PCI to PCI-Bridge
FEBFC000	FEBFFFFF	16384	Marvell Yukon 88E8055 PCI-E Gigabit Ethernet
FEC00000	FEC00FFF	4096	Motherboard resources
FEC00000	FFFFFFFF	20971520	System board
FEC10000	FEC1001F	32	Motherboard resources
FED00000	FED003FF	1024	High precision event timer
FEE00000	FEE00FFF	4096	Motherboard resources
FFB80000	FFBFFFFF	524288	Motherboard resources

Notes: This is the memory map after a standard Windows XP SP2 installation

5.1.1 PCI devices

Bus #	Device #	Function #	Vendor ID	Device ID	IDSEL	Chip	Device Function
0	0	0	1022h	9600h		SB700	Host bridge
0	1	0	1022h	9602h		SB700	Pci to Pci Brigde
0	9	0	1022h	9608h		SB700	Pci to Pci Brigde
0	10	0	1022h	9609h		SB700	Pci to Pci Brigde
0	17	0	1002h	4390h		SB700	IDE Controller
0	18	0	1002h	4397h		SB700	USB
0	18	1	1002h	4398h		SB700	USB
0	18	2	1002h	4396h		SB700	USB
0	19	0	1002h	4397h		SB700	USB
0	19	1	1002h	4398h		SB700	USB
0	19	2	1002h	4396h		SB700	USB
0	20	0	1002h	4385h		SB700	SMBus
0	20	1	1002h	439Ch		SB700	IDE Controller
0	20	2	1002h	4383h		SB700	HD Audio
0	20	3	1002h	439Dh		SB700	ISA Bridge
0	20	4	1002h	4384h		SB700	Pci to Pci Brigde
0	20	5	1002h	4399h		SB700	USB
0	24	0	1022h	1200h		SB700	Host bridge
0	24	1	1022h	1201h		SB700	Host bridge
0	24	2	1022h	1202h		SB700	Host bridge
0	24	3	1022h	1203h		SB700	Host bridge
0	24	4	1022h	1204h		SB700	Host bridge
1	5	0	1002h	9610h		SB780	VGA Controller
1	5	1	1002h	960Fh		SB700	HD Audio
2	0	0	11ABh	4363h		Marvell 88E8055	Ethernet
3	0	0	11ABh	4363h		Marvell 88E8055	Ethernet
4	5		-	-		-	PCI Slot 1
4	6		-	-		-	PCI Slot 2
4	7		-	-		-	PCI Slot 3
4	8		-	-		-	PCI Slot 4
			-	-		-	PCI-E Slot 4x
			-	-		-	PCI-E Slot 16x

When a PCI-E card is used it could change the BUS number on other PCI-E and PCI devices like RTL8111b.
Note: PCI slot supports PCI BUS Mastering.

5.2 Interrupt Usage

IRQ	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port A	May be used by onboard Serial Port B / IrDA Port	May be used by onboard Parallel Port	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used for SATA RAID controller	May be used for onboard Sound System	May be used for PCI Express Root Port	May be used by onboard USB controller	May be used by onboard Ethernet controller 1	May be used by onboard Ethernet controller 2	May be used by onboard VGA Controller	May be used by onboard IDE Controller	May be used by Microsoft ACPI-Compliant System	Available on PCI slots as IRQA-IRQD	Notes
NMI	•										?										
IRQ0		•																			
IRQ1			•																		
IRQ2				•																	
IRQ3						•															1, 2
IRQ4					•																1, 2
IRQ5																				•	1, 2
IRQ6																					1, 2
IRQ7							•													•	1, 2
IRQ8								•													
IRQ9																			•	•	1, 2
IRQ10																				•	1, 2
IRQ11																				•	1, 2
IRQ12									•												1
IRQ13										•											
IRQ14																					1
IRQ15																					1
IRQ16												•		•							3
IRQ17														•		•					3
IRQ18														•	•		•				3
IRQ19												•		•							3
IRQ20																					3
IRQ21																					3
IRQ22																		•			3
IRQ23																					3
IRQ24																					3
IRQ25																					3
IRQ26																					3

Notes:

1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQD can be shared.
2. These IRQ´s are managed by the PnP handler and are subject to change during system initialization.
3. IRQ16 to IRQ26 are APIC interrupts
4. This is the IRQ map after a standard Windows XP SP2 installation

5.3 I/O Map

Address (hex)		Size	Description
00000000	0000000F		DMA-controller
00000000	00000CF7		PCI-bus
00000010	0000001F		Motherboard resources
00000020	00000021		Programmable interrupt controller
00000022	0000003F		Motherboard resources
00000040	00000043		Systemtimer
00000060	00000060		Standard Keyboard
00000061	00000061		System speaker
00000062	00000063		Motherboard resources
00000064	00000064		Standard Keyboard
00000065	0000006F		Motherboard resources
00000070	00000071		System CMOS/Real time clock
00000072	0000007F		Motherboard resources
00000080	00000080		Motherboard resources
00000081	00000083		DMA-controller
00000084	00000086		Motherboard resources
00000087	00000087		DMA-controller
00000088	00000088		Motherboard resources
00000089	0000008B		DMA-controller
0000008C	0000008E		Motherboard resources
0000008F	0000008F		DMA-controller
00000090	0000009F		Motherboard resources
000000A0	000000A1		Programmable interrupt controller
000000A2	000000BF		Motherboard resources
000000B1	000000B1		Motherboard resources
000000C0	000000DF		DMA-controller
000000E0	000000EF		Motherboard resources
000000F0	000000FF		Numeric data processor
00000170	00000177		Secondary IDE Channel
000001F0	000001F7		Primary IDE Channel
00000274	00000279		ISAPNP Read Data Port
000002F8	000002FE		ISAPNP Read Data Port
000002F8	000002FF		COM2
00000376	00000376		Secondary IDE Channel
00000378	0000037F		LPT1
000003B0	000003BB		ATI Radeon HD 3200 Graphics
000003B0	000003BB		PCI-to-PCI bridge
000003C0	000003DF		ATI Radeon HD 3200 Graphics
000003C0	000003DF		PCI-to-PCI bridge
000003F6	000003F6		Primary IDE Channel
000003F8	000003FF		Com1
000003F8	000003FF		Motherboard resources
0000040B	0000040B		Motherboard resources
000004D0	000004D1		Motherboard resources
000004D6	000004D6		Motherboard resources
00000800	0000089F		Motherboard resources
00000900	0000090F		Motherboard resources
00000910	0000091F		Motherboard resources
00000A79	00000A79		ISAPNP Read Data Port
00000B00	00000B0F		Motherboard resources

00000B20	00000B3F		Motherboard resources
00000C00	00000C01		Motherboard resources
00000C14	00000C14		Motherboard resources
00000C50	00000C51		Motherboard resources
00000C52	00000C52		Motherboard resources
00000C6C	00000C6C		Motherboard resources
00000C6F	00000C6F		Motherboard resources
00000CD0	00000CD1		Motherboard resources
00000CD2	00000CD3		Motherboard resources
00000CD4	00000CD5		Motherboard resources
00000CD6	00000CD7		Motherboard resources
00000CD8	00000CDF		Motherboard resources
00000D00	0000FFFF		PCI-bus
00000E00	00000E0F		Motherboard resources
00000E10	00000E1F		Motherboard resources
00007000	0000700F		Standard Dual Channel PCI IDE-controller
00008000	00008003		Standard Dual Channel PCI IDE-controller
00009000	00009007		Standard Dual Channel PCI IDE-controller
0000A000	0000A003		Standard Dual Channel PCI IDE-controller
0000B000	0000B007		Standard Dual Channel PCI IDE-controller
0000C000	0000C0FF		ATI Radeon HD 3200 Graphics
0000C000	0000CFFF		PCI-to-PCI bridge
0000D000	0000DFFF		PCI-to-PCI bridge
0000D800	0000D8FF		Marvell Yukon 88E8055 PCI-E Gigabit Ethernet 1
0000E000	0000EFFF		PCI-to-PCI bridge
0000E800	0000E8FF		Marvell Yukon 88E8055 PCI-E Gigabit Ethernet 2
0000FE00	0000FEFE		Motherboard resources
0000FF00	0000FF0F		Standard Dual Channel PCI IDE-controller

Notes: This is the IO map after a standard Windows XP SP2 installation

5.4 DMA Channel Usage

DMA Channel Number	Data Width	System Resources
0	8 or 16 bits	Available
1	8 or 16 bits	Available
2	8 or 16 bits	Available
3	8 or 16 bits	Available
4	8 or 16 bits	DMA Controller
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

6. Overview of BIOS features

This Manual section details specific BIOS features for the KT780/ATX boards.
The KT780/ATX boards are based on the AMI BIOS core version 8.10 with Kontron BIOS extensions.

6.1 System Management BIOS (SMBIOS / DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:
• BIOS data, such as the BIOS revision level
• Fixed-system data, such as peripherals, serial numbers, and asset tags
• Resource data, such as memory size, cache size, and processor speed
• Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

6.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

7. BIOS Configuration / Setup

7.1 Introduction

The BIOS Setup is used to view and configure BIOS settings for the KT780/ATX board. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The Menu bar look like this:

```
BIOS SETUP UTILITY
Main  Advanced  PCIPnP  Boot  Security  Chipset  Exit
```

The available keys for the Menu screens are:

Select Menu: <←> or <→>
Select Item: <↑> or <↓>
Select Field: <Tab>
Change Field: <+> or <->
Help: <F1>
Save and Exit: <F10>
Exits the Menu: <Esc>

Please note that in the following the different BIOS Features will be described as having some options. These options will be selected automatically when loading either Failsafe Defaults or Optimal Defaults. The Default options will be indicated by the option in bold, but please notice that when Failsafe Defaults are loaded a few of the options, marked with "*", are now the default option.

7.2 Main Menu

```
BIOS SETUP UTILITY
   Main   Advanced   PCIPnP   Boot   Security   Chipset   Exit

AMIBIOS                                    | Use [ENTER], [TAB] or
ID        : KT780012                       | [SHIFT-TAB] to select
Build Date: 10/01/09                       | a field.
PCB ID    : 0B                             |
Serial #  : 00615444                       | Use [+] or [-] to
Part   #  : 61810000                       | configure system Time.
                                           |
Processor                                  |
AMD Athlon(tm) 64 Processor 2600+          |
Speed     : 1600MHz                        |
Count     : 1                              | <-   Select Screen
                                           | ||   Select Item
System Memory                              | +-   Change Field
Size      : 896MB                          | Tab  Select Field
                                           | F1   General Help
System Time          [10:18:15]            | F10  Save and Exit
System Date          [17/09/2008]          | ESC  Exit

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```

You can make the following selections. Use the sub menus for other selections.

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.

7.3 Advanced Menu

```
                        BIOS SETUP UTILITY
       Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit

  > CPU Configuration                          Configure CPU.
  > IDE Configuration
  > LAN Configuration
  > SuperIO Configuration
  > Hardware Health Configuration
  > Voltage Monitor
  > ACPI Configuration
  > PCI Express Configuration
  > USB Configuration
  > Trusted Computing

                                               <-    Select Screen
                                               ||    Select Item
                                               Enter Go to Sub Screen
                                               F1    General Help
                                               F10   Save and Exit
                                               ESC   Exit

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```

7.3.1 Advanced settings – CPU Configuration

```
                        BIOS SETUP UTILITY
                              Advanced

  AMD Athlon(tm) 64 X2 Dual Core Processor 4600+   Enable/Disable the
  Speed     :2400Mhz,          NB CLK: N/A         Generation of ACPI
  Cache L1: 256KB                                  _PPC, _PSS, and _PCT
  Cache L2: 1024KB                                 Objects.

  PowerNow                    [Enabled]
  HAT Link Speed   :          [Auto]

                                               <-    Select Screen
                                               ||    Select Item
                                               +-    Change Option
                                               F1    General Help
                                               F10   Save and Exit
                                               ESC   Exit

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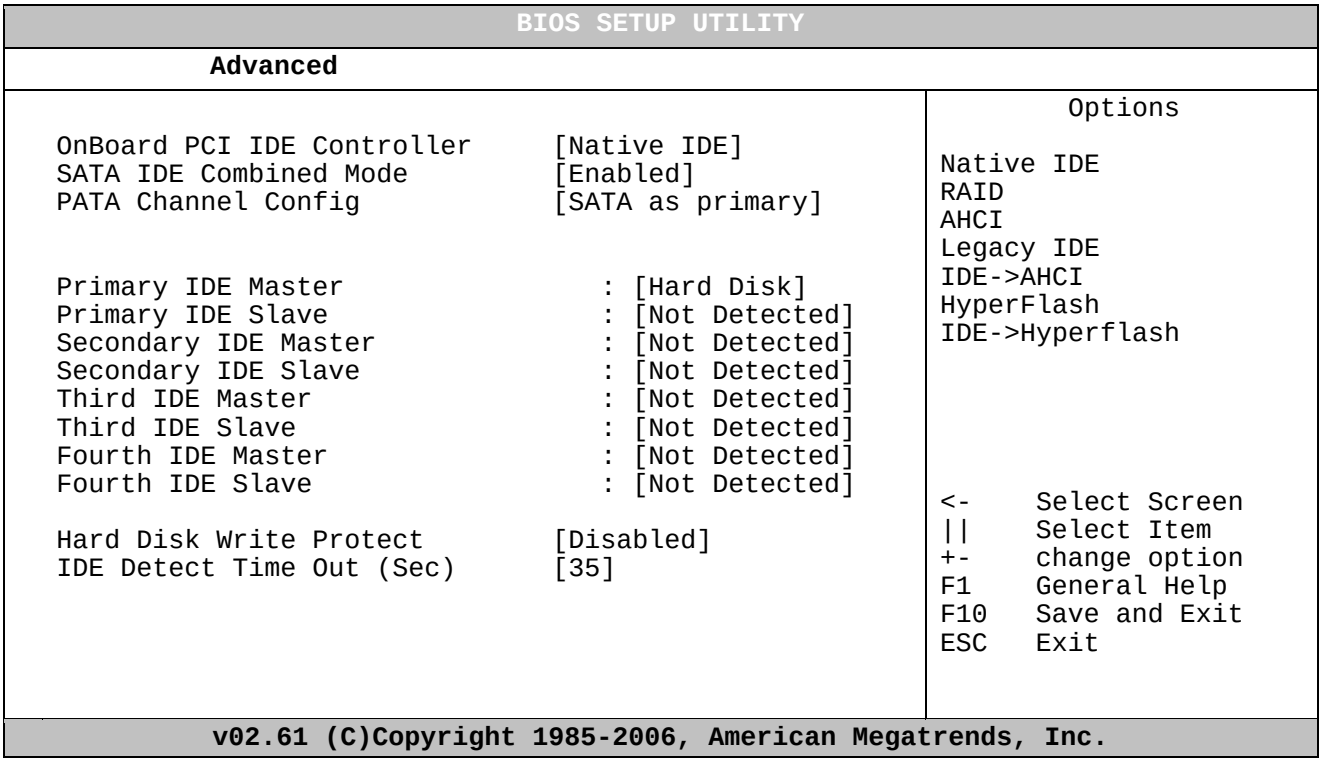
Feature	Options	Description
PowerNow	**Enabled** Disabled	Enable/Disable the Generation of ACPI _PPC, _PSS, and _PCT objects
HAT Link Speed	200 Mhz 400 Mhz 600 Mhz 800 Mhz 1 Ghz **Auto**	The hyperTransport link will run at this speed if it is slower than or equal to the system clock and the board is capable.

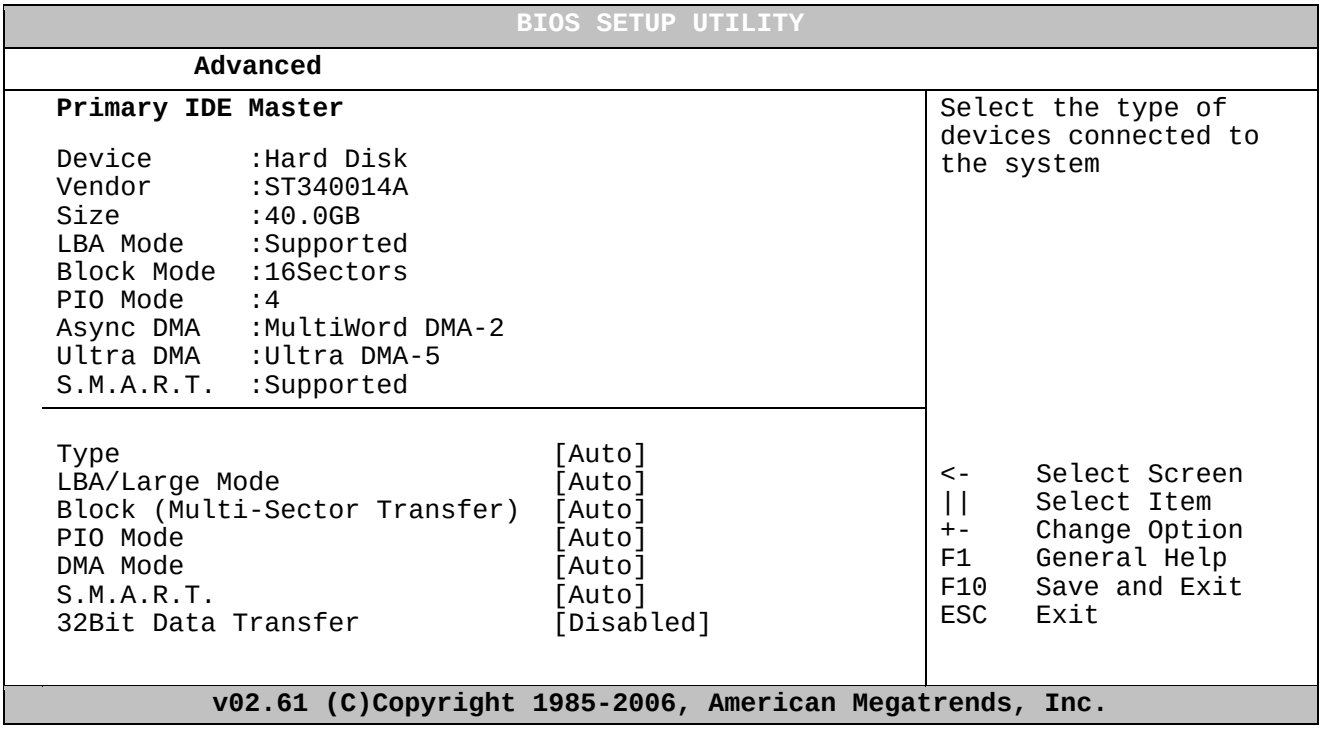
7.3.2 Advanced settings – IDE Configuration



Feature	Options	Description
OnBoard PCI IDE Controller	**Native IDE** RAID AHCI Legacy IDE IDE->AHCI HyperFlash IDE->Hyperflash	Native IDE RAID AHCI Legacy IDE IDE->AHCI HyperFlash IDE->Hyperflash

Feature	Options	Description
SATA IDE Combined Mode	**Enabled** Disabled	Enabled: note, required for using SATA port 5 & 6. Disabled
PATA Channel Config	**SATA as Primary** SATA as secondary	SATA as Primary SATA as secondary

Feature	Options	Description
Hard Disk Write Protect	**Disabled** Enabled	Disabled Enhanced
IDE Detect Time Out (Sec)	0 5 10 15 20 25 30 **35**	Select the time out value for detecting ATA/ATAPI device(s)

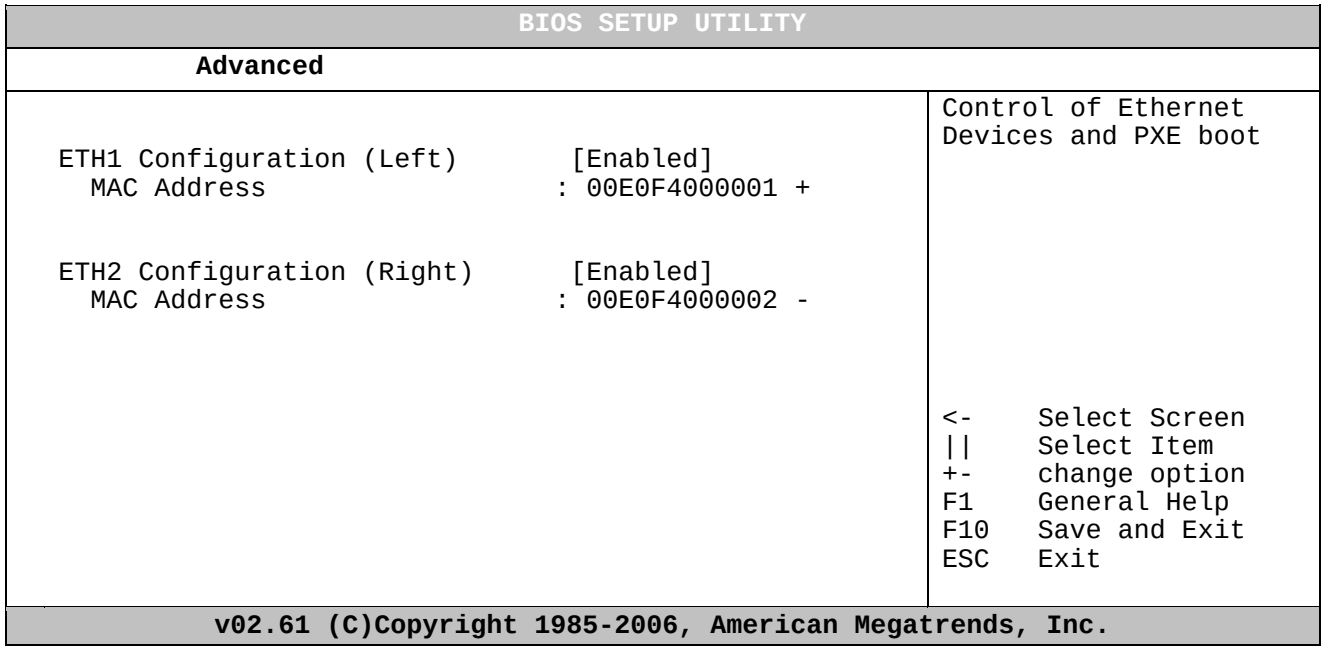


Feature	Options	Description
Type	Not Installed **Auto** CDROM ARMD	Select the type of device installed
LBA/Large Mode	Disabled **Auto**	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors.
Block (Multi-Sector Transfer)	Disabled **Auto**	Select if the device should run in Block mode
PIO Mode	**Auto** 0 1 2 3 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **Note: To use UDMA Mode 2, 3, 4 and 5 with a device, the harddisk cable used MUST be UDMA66/100 cable (80-conductor cable).**
S.M.A.R.T.	**Auto** Disabled Enabled	Select if the Device should be monitoring itself (Self-Monitoring, Analysis and Reporting Technology System)
32Bit Data Transfer	**Disabled** Enabled	Select if the Device should be using 32Bit data Transfer

(continues)

Feature	Options	Description
Hard Disk Write Protect	**Disabled** Enabled	Enable write protection on HDDs, only works when it is accessed through the BIOS
IDE Detect Time Out (Sec)	0 5 10 15 20 25 30 **35**	Select the time out value when the BIOS is detecting ATA/ATAPI Devices
ATA(PI) 80Pin Cable Detection	**Host & Device** Host Device	Select the mechanism for detecting 80Pin ATA (PI) Cable

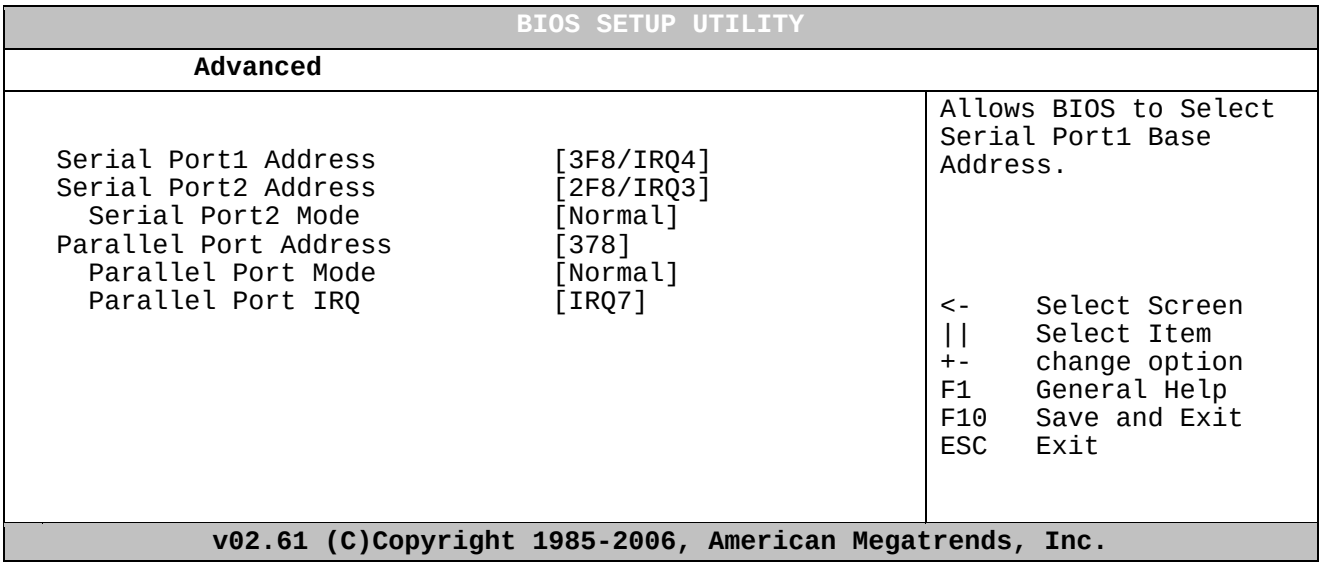
7.3.3 Advanced settings – LAN Configuration



Feature	Options	Description
ETH1 Configuration	Disabled **Enabled** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom
ETH2 Configuration	Disabled **Enabled** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom

Note: The “+” and “-“ (to the right of the MAC address) indicates if link is established or not.

7.3.4 Advanced settings – Super IO Configuration



Feature	Options	Description
Serial Port1 Address	Disabled **3F8/IRQ4** 3E8/IRQ4 3E8/IRQ3	Select the BASE I/O address and IRQ. (The available options depends on the setup for the other Serial Ports).
Serial Port2 Address	Disabled **2F8/IRQ3** 3E8/IRQ4	Select the BASE I/O address and IRQ. (The available options depends on the setup for the other Serial Ports).
Serial Port2 Mode	**Normal** IRDA ASK IR	Select Mode for Serial Port2
Parallel Port Address	Disabled ***** **378** 278 3BC	Select the I/O address for the PRINTER.
Parallel Port Mode	**Normal** Bi-Directional ECP EPP ECP & EEP	Select the mode that the parallel port will operate in
EPP Version	**1.9** 1.7	Setup with version of EPP you want to run on the parallel port
ECP Mode DMA Channel	DMA0 DMA1 **DMA3**	Select a DMA channel
Parallel Port IRQ	IRQ5 **IRQ7**	Select a IRQ

7.3.5 Advanced settings – Hardware Health Configuration

```
                         BIOS SETUP UTILITY
                              Advanced
                                                  Disable = Full Speed.

  Ambient                      :37°C/98°F          Thermal: Does regulate
  CPU Temperature              :43°C/109°F         fan speed according to
  TEMP3IN  Temperature         :N/A                specified temperature

  SystemFan Speed              :N/A                Speed: Does regulate
    Fan Cruise Control            [Disabled]       according to specified
    Fan Type                      [4 Wire]         RPM.
  CPUFan Speed                 :2537 RPM
    Fan Cruise Control            [Thermal]
    Fan Setting                   [45°C/113°F]
    Fan Type                      [4 Wire]
  Fan3 Speed                 :2164
    Fan Cruise Control            [Speed]
    Fan Setting                   [2177 RPM]       <-    Select Screen
  IOFAN Speed                  :N/A                ||    Select Item
    Fan Cruise Control            [Disabled]       +-    change option
    Fan Type                      [4 Wire]         F1    General Help
                                                   F10   Save and Exit
  Watchdog Function               [Disabled]       ESC   Exit

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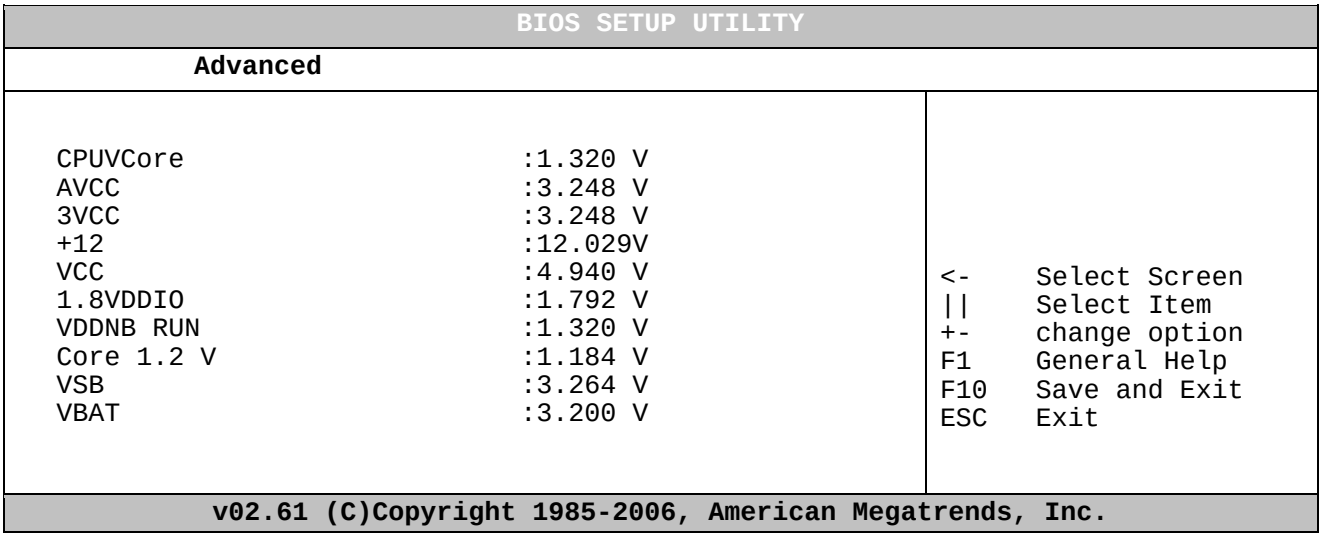
```

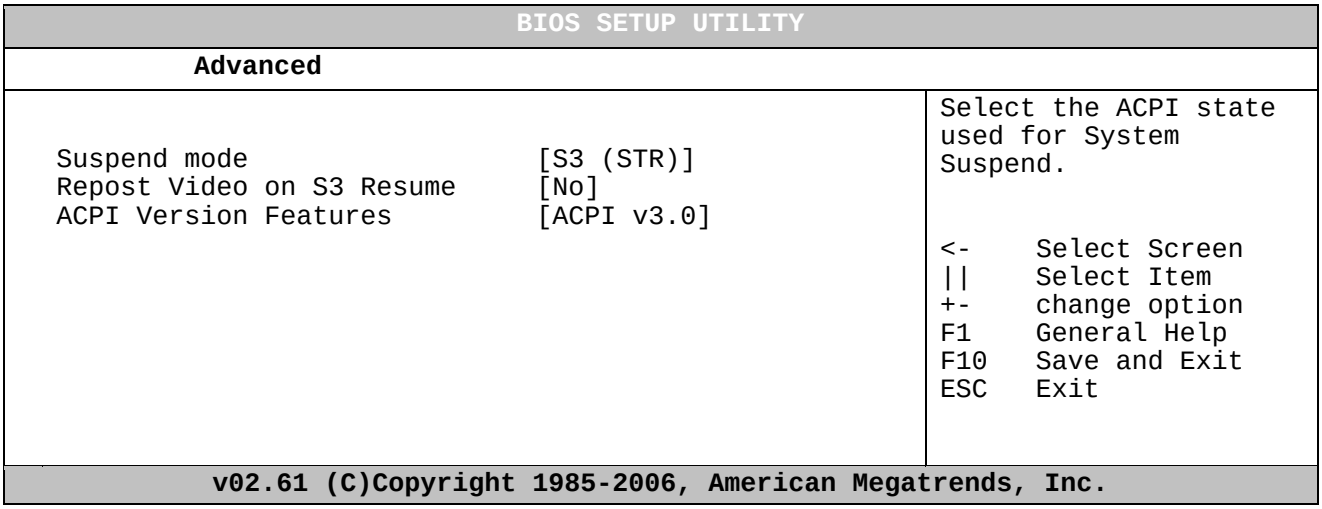
Feature	Options	Description
Fan Cruise Control	**Disabled** Thermal Speed	Select how the Fan shall operate. When set to Thermal, the Fan will start to run at the CPU die temperature set below. When set to Speed, the Fan will run at the Fixed speed set below.
Fan Type	**4 wire** 3 wire	Select the electrical interface for the fan: 3 Wire = PWM output to fan power line. RPM reading and speed regulation at lower speed might be poor. 4 Wire = 12VDC always PWM on control signal
Fan Settings	1406-5625 RPM 30°-60°C	The fan can operate in Thermal mode or in a fixed fan speed mode
Watchdog	**Disabled** 15 seconds 30 seconds 1 minute 2 minutes 5 minutes 10 minutes	To be serviced via API.

Note: Fan3 is the same as the FAN_NB and it only has 3 pin, so that no 3 Wire/4 Wire selection is available.

7.3.6 Advanced settings – Voltage Monitor



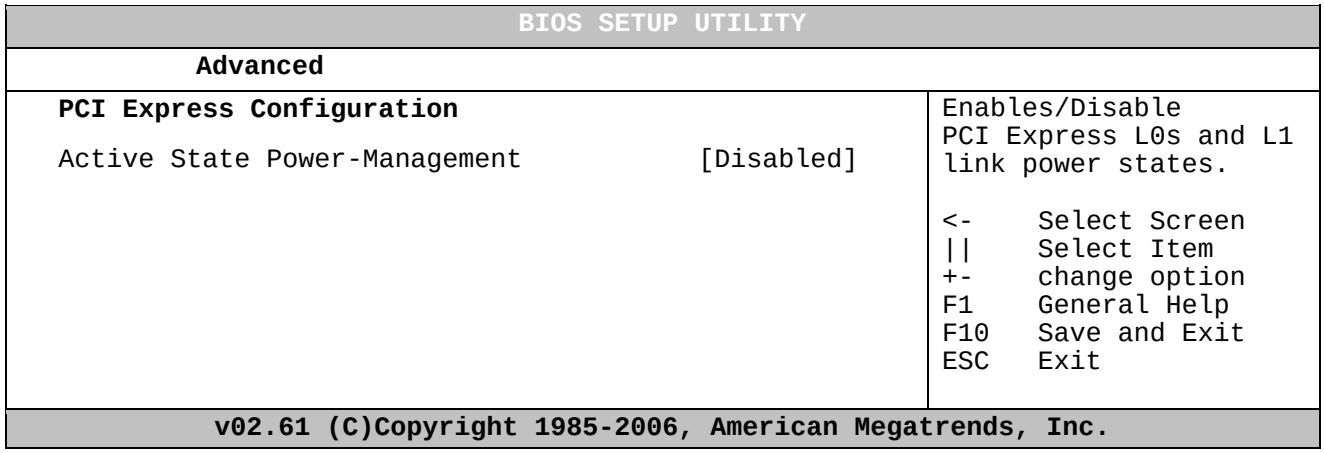
7.3.7 Advanced settings – ACPI Configuration



Advanced ACPI Configuration

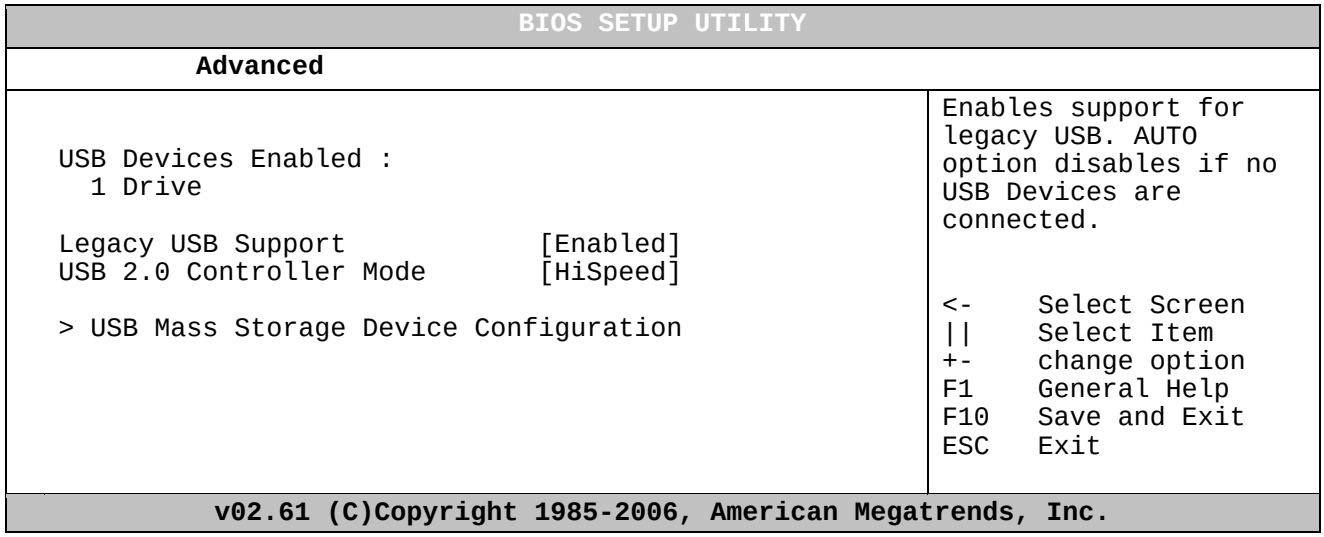
Feature	Options	Description
Suspend mode	S1 (POS) * **S3 (STR)** Auto	Select the ACPI state used for System Suspend
Repost Video on S3 Resume	**No** Yes	Determines whether to invoke VGA BIOS post on S3/STR resume
ACPI Version Features	ACPI v1.0 ACPI v2.0 **ACPI v3.0**	Enable RSDP pointers to 64-bit Fixed System Description Tables. Di ACPI version has some.

7.3.8 Advanced settings – PCI Express Configuration



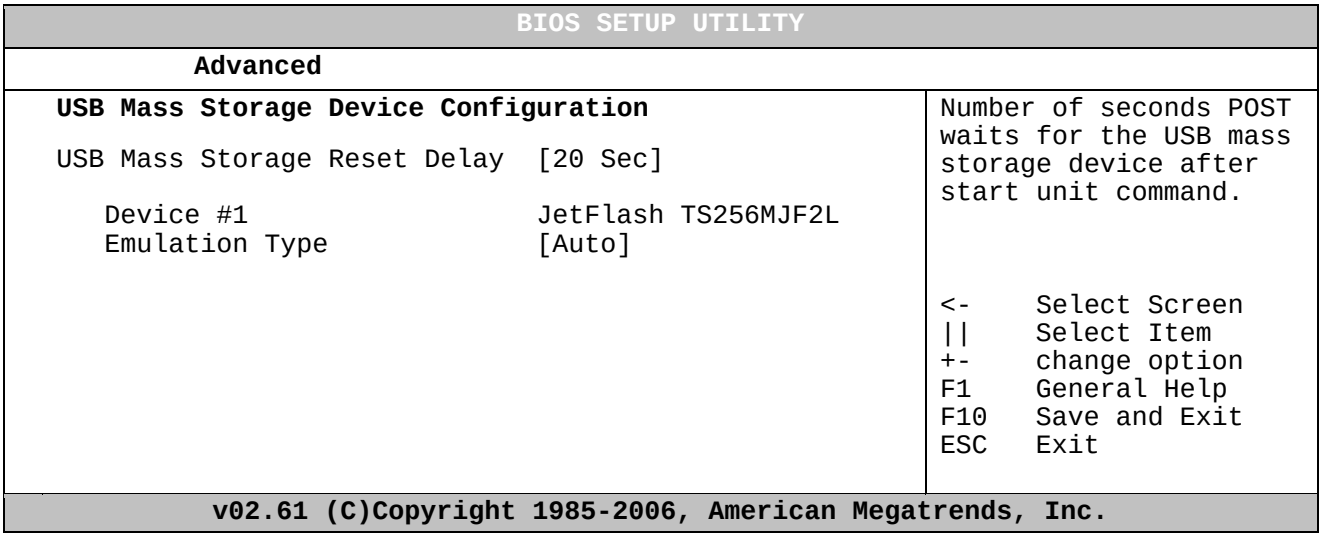
Feature	Options	Description
Active State Power-Management	**Disabled** Enabled	Enables/Disable. PCI Express L0s and L1 link power states

7.3.9 Advanced settings – USB Configuration



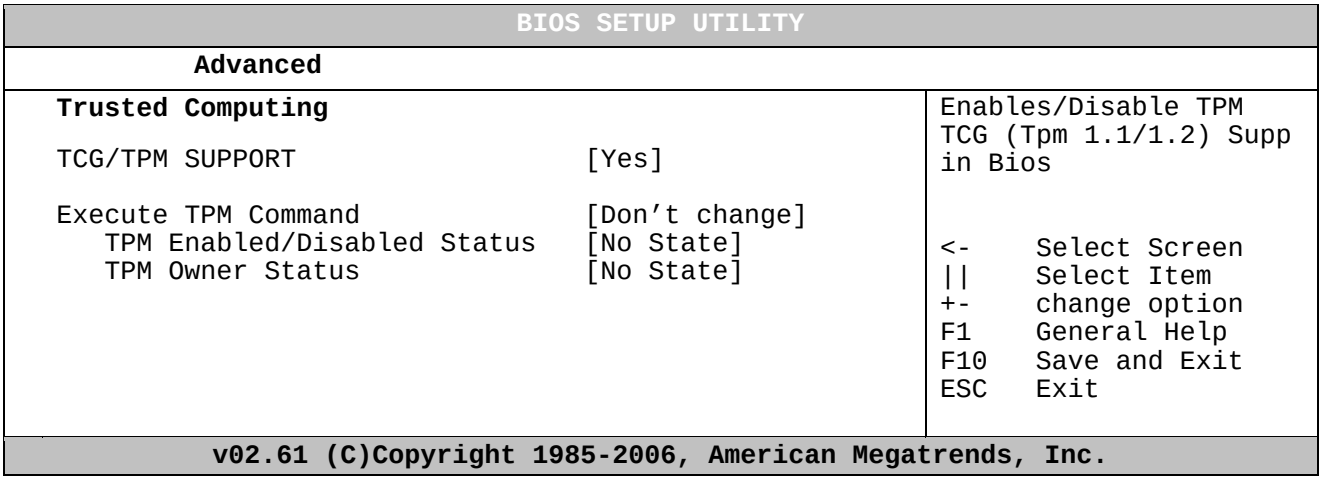
Feature	Options	Description
Legacy USB Support	Disabled **Enabled** Auto	Support for legacy USB Keyboard
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configure the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps). Note: This feature is not available when Failsafe Defaults are loaded, because USB2.0 controller is disabled as default.
BIOS EHCI Hand-Off	Enabled **Disabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI Ownership change should claim by EHCI driver.

7.3.10 Advanced settings – USB Mass Storage Device Configuration



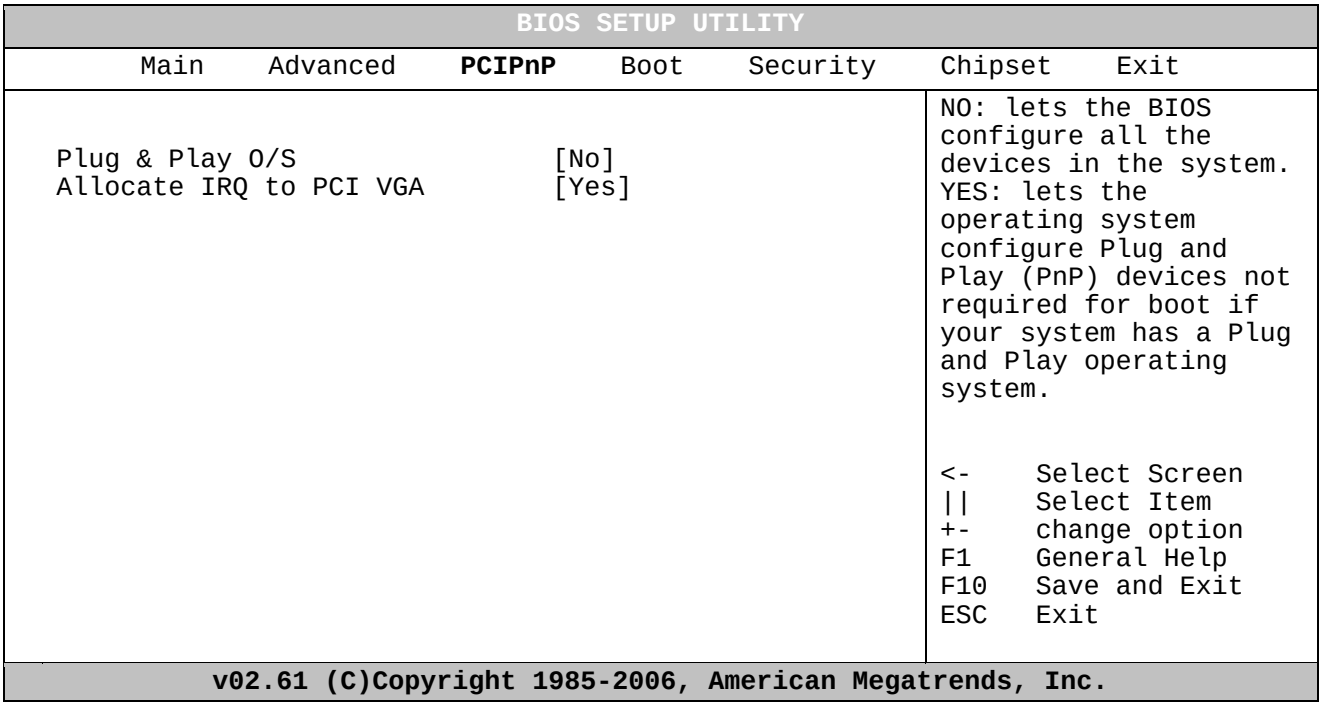
Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

7.3.11 Advanced settings – Trusted Support



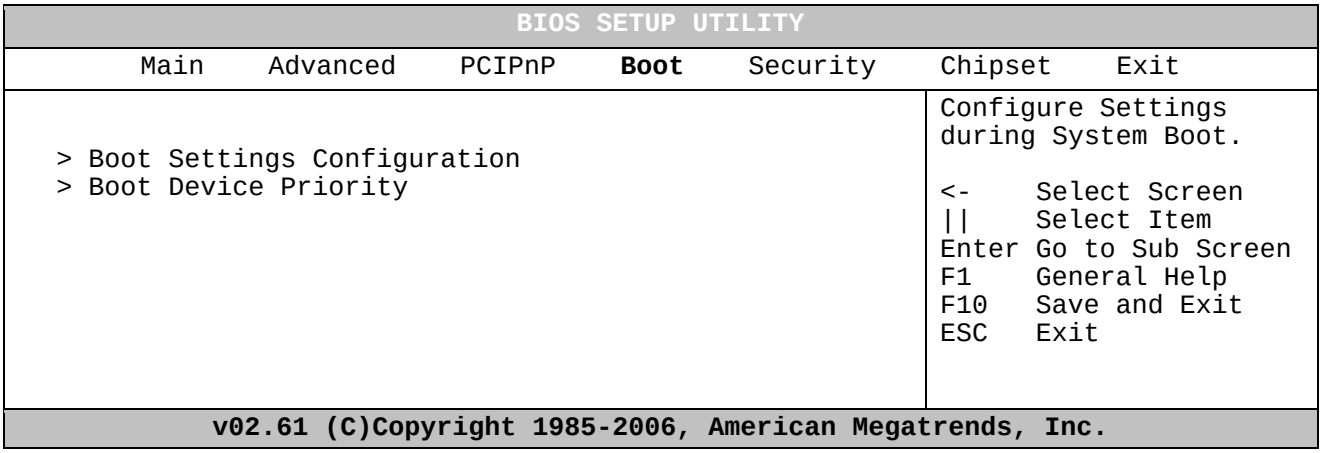
Feature	Options	Description
TCG/TPM SUPPORT	**No** Yes	Enables/Disable TPM TCG (TPM 1.1/1.2) Support.
Execute TPM Command	**Don't change** Disabled Enabled	Enable(Activate)/ Disable(Deactivate) Command to TPM

7.4 PCIPnP Menu

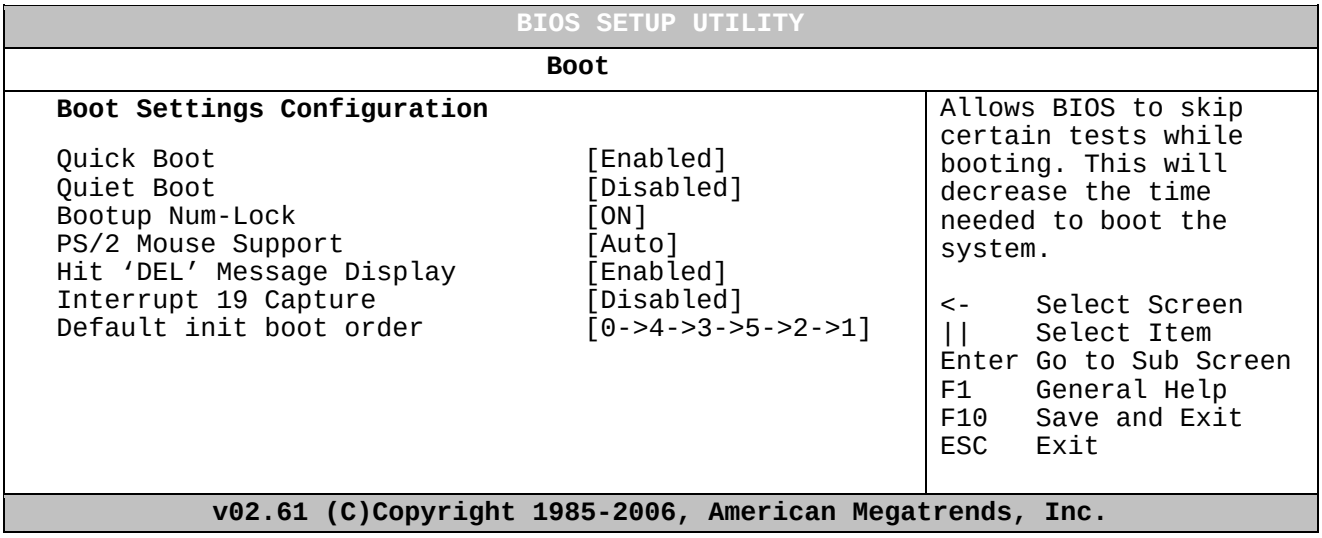


Feature	Options	Description
Plug & Play O/S	**No *** Yes	NO: lets the BIOS configure all the devices in the system. YES: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.
IRQ	**Yes** No	YES: Assigns IRQ to PCI VGA card if card requests IRQ. No: Does not assign IRQ to PCI VGA card even if card requests an IRQ.

7.5 Boot Menu


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
> Boot Settings Configuration
> Boot Device Priority
Configure Settings during System Boot.
<- Select Screen
|| Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

7.5.1 Boot – Boot Settings Configuration



Feature	Options	Description
Quick Boot	**Enabled** Disabled	Allows BIOS to skip certain test while booting in order to decrease boot time.
Quiet Boot	**Disabled** Enabled	Disabled: Displays normal POST messages. Enabled: Displays OEM Logo (no POST messages).
Bootup Num-Lock	Off **On**	Select Power-on state for numlock
PS/2 Mouse Support	Disabled Enabled **Auto**	Select support for PS/2 Mouse.
Hit 'DEL' Message Display	Disabled **Enabled**	Displays "Press DEL to run Setup" in POST.
Interrupt 19 Capture	**Disabled** Enabled	Enabled: Allows option ROMs to trap interrupt 19
Default init boot order	**0->4->3->5->2->1** 0->4->3->5->1->2 1->2->3->5->0->4 3->5->1->2->0->4 3->0->4->1->2->5 2->1->0->4->3->5 2->0->4->3->1->5 3->1->0->4->2->5	The numbers in the sequence means: 0 = "Removables" 1 = "Hard Disk" 2 = "ATAPI CDROM" 3 = "BEV/onboard LAN" 4 = "USB" 5 = "External LAN"

Note: List of errors:

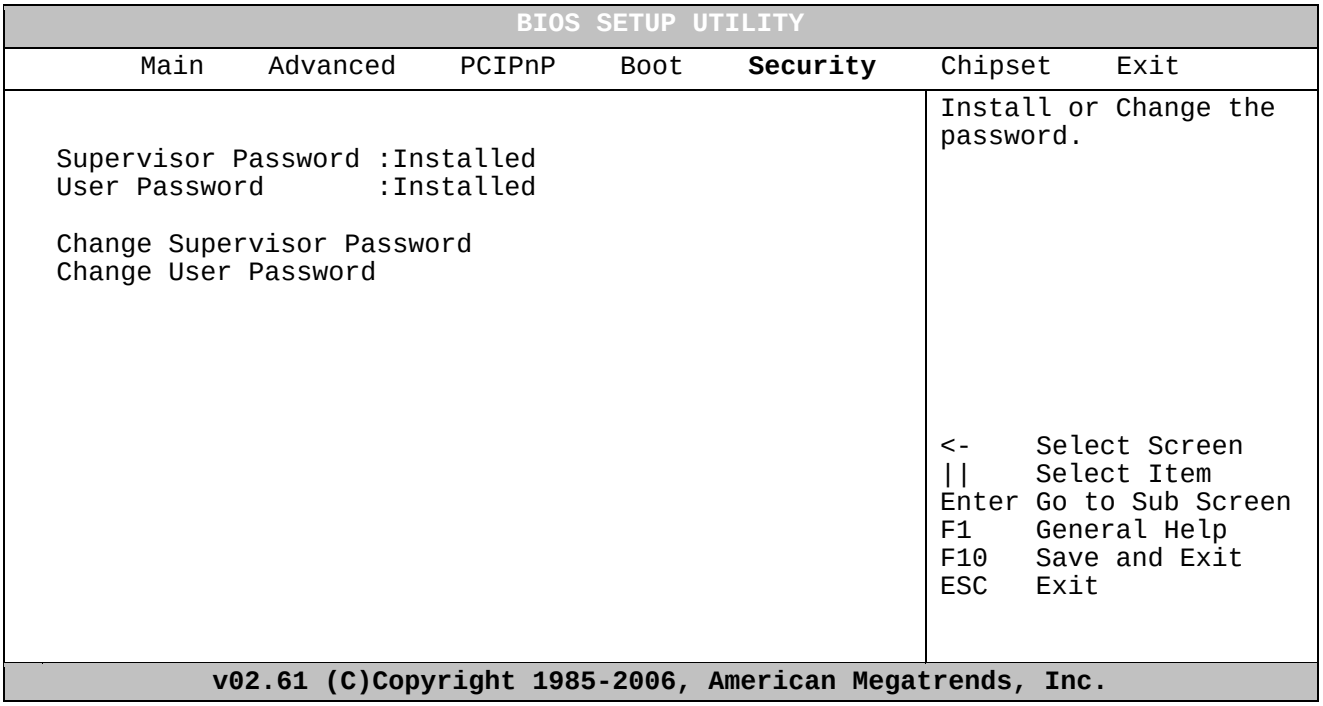
<INS> Pressed
Timer Error
Interrupt Controller-1 error
Keyboard/Interface Error
Halt on Invalid Time/Date
NVRAM Bad
Primary Master Hard Disk Error
S.M.A.R.T HDD Error
Cache Memory Error
DMA Controller Error
Resource Conflict
Static Resource Conflict
PCI I/O conflict
PCI ROM conflict
PCI IRQ conflict
PCI IRQ routing table error

7.5.2 Boot – Boot Device Priority

BIOS SETUP UTILITY	
Boot	
Boot Device Priority 1st Boot Device [ESS-ST380811AS]	Specifies the boot sequence from the available devices. A device enclosed in parenthesis has been disabled in the corresponding type menu. <- Select Screen || Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.	

Note: When pressing <F11> while booting it is possible manually to select boot device.

7.6 Security Menu



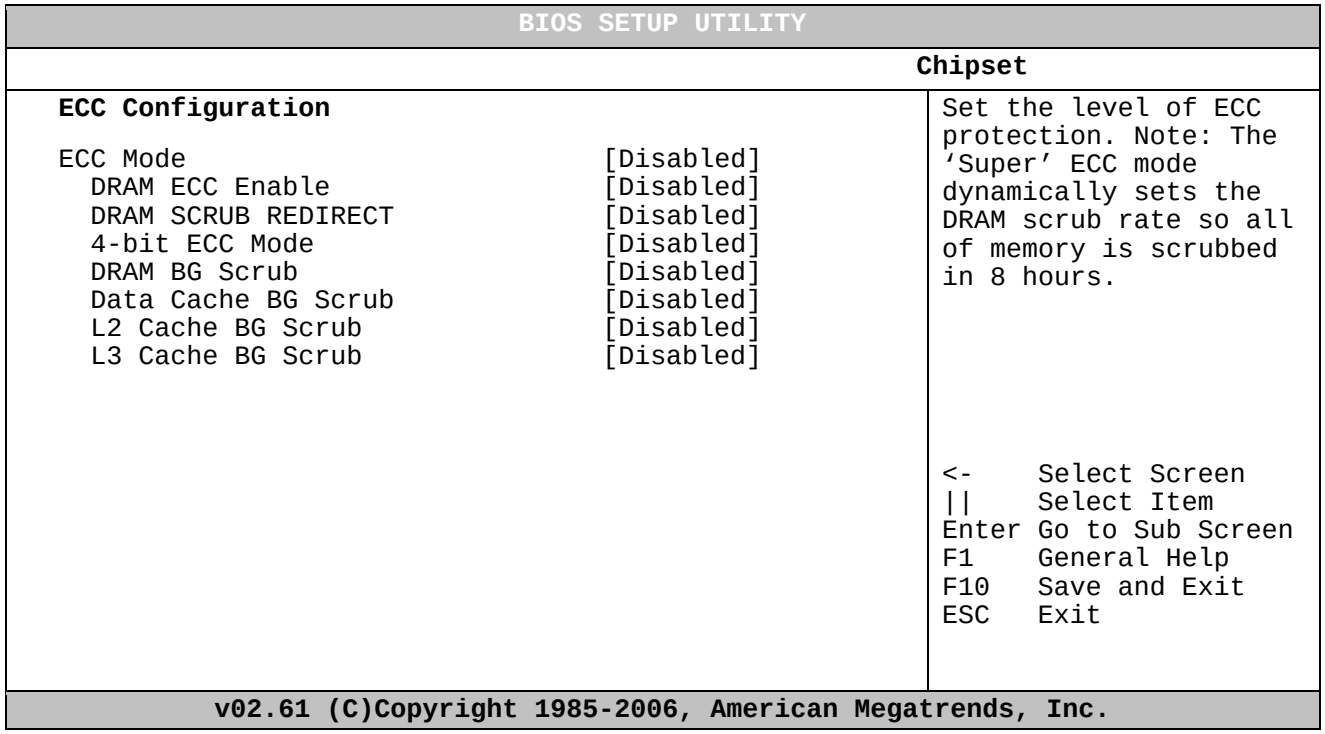
Feature	Options	Description
Change Supervisor Password	Password	Change the Supervisor Password
Change User Password	Password	Change the User Password

7.7 Chipset Menu

BIOS SETUP UTILITY	
Main Advanced PCIPnP Boot Security **Chipset** Exit	
> NorthBridge Configuration > Video function Configuration > SouthBridge Configuration	Option for NB <- Select Screen || Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.	

7.7.1 Advanced Chipset Settings – North Bridge Chipset Configuration

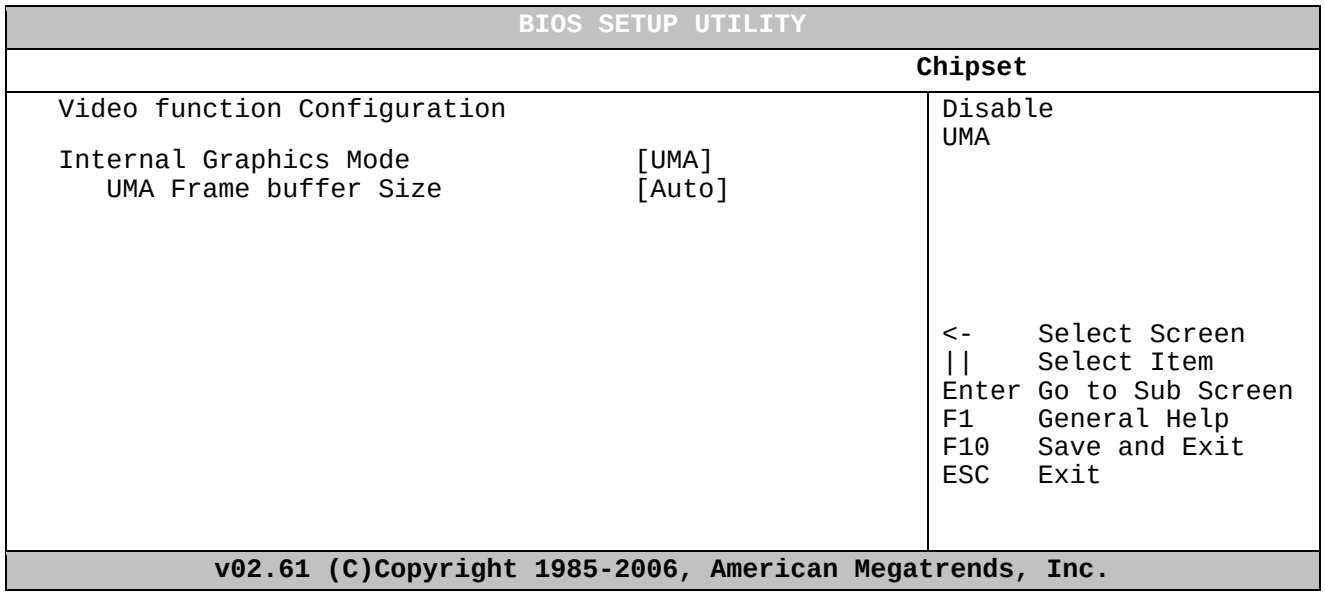
BIOS SETUP UTILITY	
Chipset	
North Bridge Chipset Configuration > ECC Configuration Primary Video Controller [GFX0-GPP-IGFX-PCI] VBIOS :DVI	Set the ECC options for cache and dram scrubbing <- Select Screen || Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.	



Feature	Options	Description
ECC Mode	**Disabled** Basic Good Super Max User	Set the level of ECC protection. Note: The 'Super' ECC mode dynamically sets the DRAM scrub rate so all of memory is scrubbed in 8 hours.
DRAM ECC Enable	**Disabled** Enabled	Only manual selectable when ECC Mode is User.
DRAM SCRUB REDIRECT	**Disabled** Enabled	Only manual selectable when ECC Mode is User.
4-bit ECC Mode	**Disabled** Enabled	Only manual selectable when ECC Mode is User.
DRAM BG Scrub	**Disabled** "2^N x 40ns (N = 0–14)"	Only manual selectable when ECC Mode is Max or User.
Data Cache BG Scrub	**Disabled** "2^N x 40ns (N = 0–14)"	Only manual selectable when ECC Mode is User.
L2 Cache BG Scrub	**Disabled** "2^N x 40ns (N = 0–14)"	Only manual selectable when ECC Mode is User.
L3 Cache BG Scrub	**Disabled** "2^N x 40ns (N = 0–14)"	Only manual selectable when ECC Mode is User.

Feature	Options	Description
Primary Video Controller	**GFX0-GPP-IGFX-PCI** GPP-GFX0-IGFX-PCI PCI-GFX0-GPP-IGFX IGFX-GFX0-GPP-PCI	GFX0-GPP-IGFX-PCI GPP-GFX0-IGFX-PCI PCI-GFX0-GPP-IGFX IGFX-GFX0-GPP-PCI

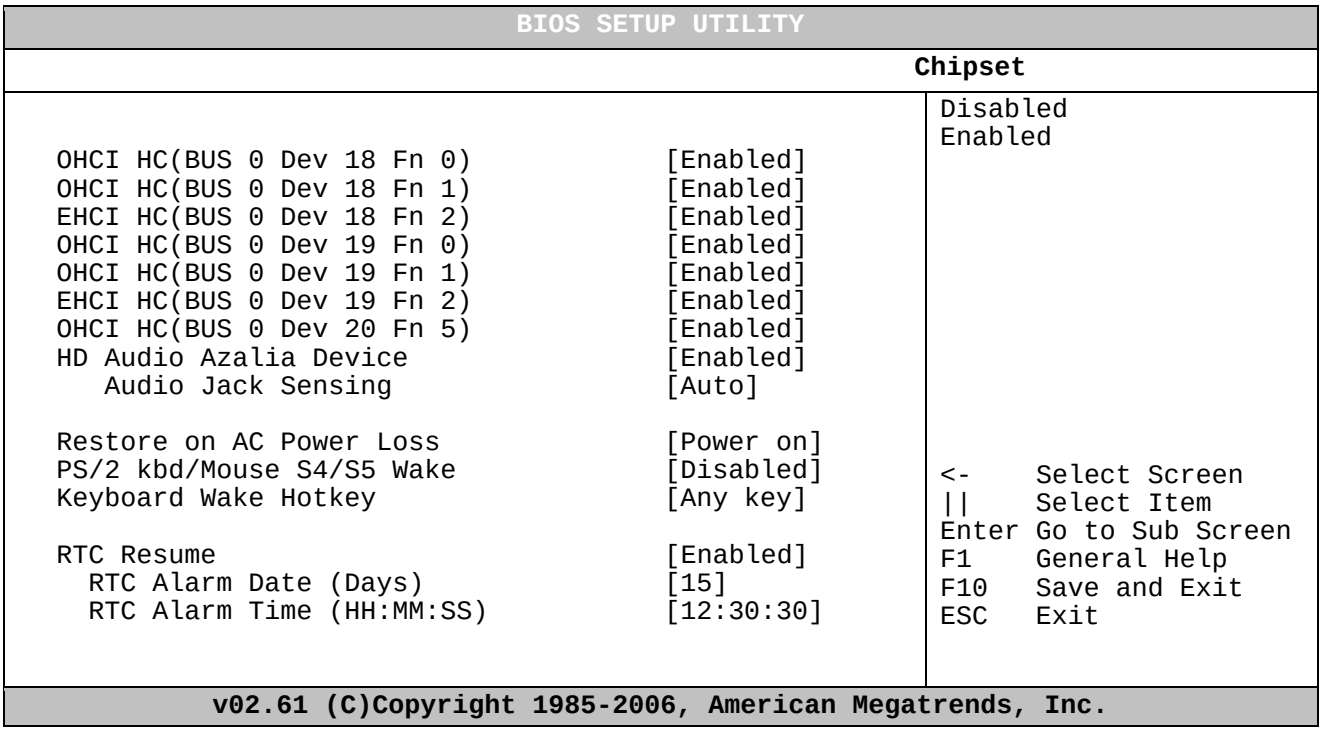
7.7.2 Advanced Chipset Settings – Video function Configuration



Video function Configuration

Feature	Options	Description
Internal Graphics Mode	Disable **UMA**	Disable UMA
UMA Frame buffer Size	**Auto** 32Mb 64MB 128MB 256MB 512MB	Auto 32Mb 64MB 128MB 256MB 512MB

7.7.3 Advanced Chipset Settings – SouthBridge Configuration



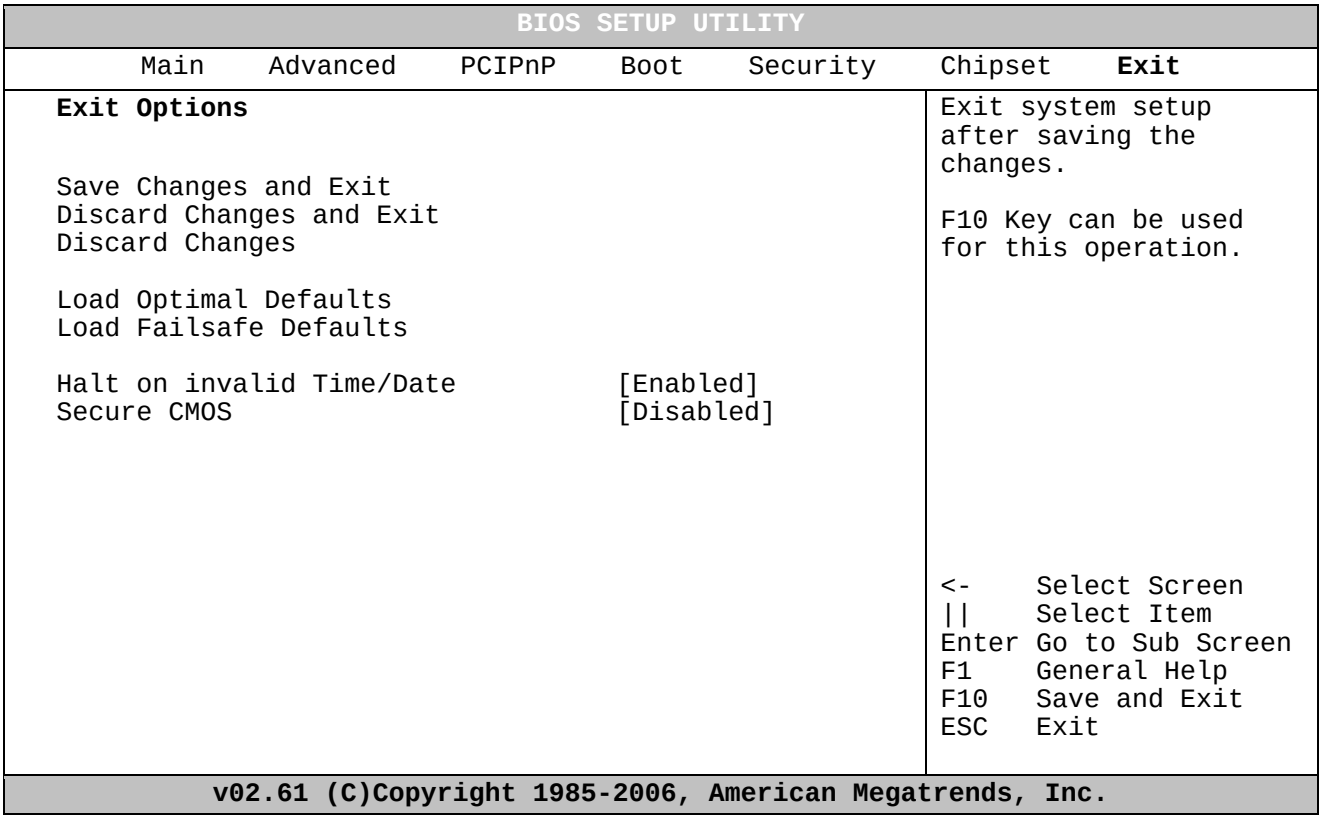
Feature	Options	Description
OHCI HC(BUS 0 Dev 18 Fn 0)	**Enabled** Disabled	Enable Disabled
OHCI HC(BUS 0 Dev 18 Fn 1)	**Enabled** Disabled	Enable Disabled
EHCI HC(BUS 0 Dev 18 Fn 2)	**Enabled** Disabled	Enable Disabled
OHCI HC(BUS 0 Dev 19 Fn 0)	**Enabled** Disabled	Enable Disabled
OHCI HC(BUS 0 Dev 19 Fn 1)	**Enabled** Disabled	Enable Disabled
EHCI HC(BUS 0 Dev 19 Fn 2)	**Enabled** Disabled	Enable Disabled
OHCI HC(BUS 0 Dev 20 Fn 5)	**Enabled** Disabled	Enable Disabled
HD Audio Azalia Device	**Enabled** Disabled	Enable Disabled: note that ATI High Def device still shown in device manager due to HDMI interface
Audio Jack sensing	**Auto** Disabled	Auto: sensing of audio jack plugs insertion is automatic. Disable, see note below.
Restore on AC Power Loss	**Power On** Power Off Last State	Power On: System reboot when AC Power turns on. Power Off: System stays off when AC Power turns on. Last State: System reboot when AC Power turns on but only if system was on when the AC Power was lost and if not coursed by Power Button activation for >4 sec.
PS/2 Kbd/Mouse S4/S5 Wake	**Disabled** Enabled	Enabled: The system can also be waked from S4 or S5. Disabled: Kbd/Mse can still wake system from S3

(continues)

Feature	Options	Description
Keyboard Wake Hotkey	**Any key** “SPACE” “ENTER” “Sleep button”	Any key “SPACE” “ENTER” “Sleep button” Note: Wakeup after Power Loss only by PS2 Kbd/Mse.
Resume On RTC Alarm	**Disabled** Enabled	Disabled/Enable RTC to generate a wake event.
RTC Alarm Date (Days)	**15**	Key In “+” / “-“ to select.
RTC Alarm Time (HH:MM:SS)	**12:30:30**	Use [ENTER], [TAB] or [SHIFT-TAB] to select a field. Use [+] or [-] to configure system Time.

Note: When sensing of audio jack plugs insertion is disabled then in Windows Open HD audio manager > Device Advance settings, the "mute front and rear devices” shall be activated. Mute rear is enabled by default when Auto sense is disabled in bios.

7.8 Exit Menu



Feature	Options	Description
Save Changes and Exit	Ok Cancel	Exit system setup after saving the changes
Discard Changes and Exit	Ok Cancel	Exit system setup without saving any changes
Discard Changes	Ok Cancel	Discards changes done so far to any of the setup questions
Load Optimal Defaults	Ok Cancel	Load Optimal Default values for all the setup questions
Load Failsafe Defaults	Ok Cancel	Load Failsafe Default values for all the setup questions
Halt on invalid Time/Date	**Enabled** Disabled	Enabled: System halt if incorrect Date & Time.
Secure CMOS	Enabled **Disabled**	Enable will store current CMOS in non volatile ram. (For protection of CMOS data in case of battery failure etc.)

8. AMI BIOS Beep Codes

Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

9. OS setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on KT780/ATX Driver CD or they can be downloaded from the homepage www.kontron.com

10. Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorized product modification, or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
   C. Causes external to the product, such as electric power fluctuations or failure.
   D. Normal wear and tear.
   E. Any other causes which does not relate to a product defect.
2. Removal, installation, and set-up service charges.

Exclusion of damages:

KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:

1. DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCONVENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS, OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.
2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.