» User Guide «

CP3002

3U CompactPCI Processor Board based on the Intel® Core™ i7 Processor with the Intel® QM57 Chipset

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Disclaimer

Table of Contents

List of Tables

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List of Figures

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Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

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Caution, Electric Shock!

Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Kontron grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

Kontron warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 Board Overview

The CP3002 is a highly integrated 3U, 4HP CompactPCI system controller board optionally expandable to 8HP and available either as a front I/O version or as a rear I/O version. It has been designed to support the multi-chip package Intel® Core™ i7 processor and the Intel® Celeron® processor in combination with the mobile Intel® QM57 Express chipset.

The board supports the Intel® Core™ i7-610E processor with 2.53 GHz frequency, the Intel® Core™ i7-620LE processor with 2.0 GHz frequency, and the Intel® Core™ i7-660UE processor with 1.33 GHz frequency, all with 64 kB L1 cache, 256 kB L2 cache and 4 MB L3 cache, as well as the Intel® Celeron® U3405 processor with 1.07 GHz frequency and 64 kB L1 cache, 512 kB L2 cache, 2 MB L3 cache. The processors are built on 32-nm technology and provided in a BGA package.

The processor is soldered on the CP3002 which results in higher Mean Time Between Failures (MTBF) and a significant improvement in cooling.

Two SODIMM sockets are available on the CP3002 to provide up to 8 GB dual-channel, third-generation Double Data Rate (DDR3) memory with Error Checking and Correcting (ECC) running at 1066 MHz. The graphics controller and the memory controller are integrated in the processor.

The board comes with two Gigabit Ethernet ports with Wake-on-LAN support (available on front I/O and switchable to rear I/O), one high-resolution VGA interface (CRT), two COM ports, as well as one onboard high-speed I/O extension connector for flexible 8HP expandability. In addition, six SATA interfaces are provided, one for the onboard SATA connector, one for the SATA Flash module, two for the high-speed I/O extension connector and two for rear I/O. Further interfaces include up to six USB 2.0 ports, two on front I/O, two on rear I/O, two for the onboard high-speed I/O extension connector. The CP3002 provides support for one 8HP I/O expansion module (CP3002-HDD) and one rear I/O module (CP-RIO3-04). The 4HP CP3002 further provides support for up to 16 GB SATA NAND flash memory (SSD) via a SATA Flash module. The SATA Flash module cannot be used in conjunction with the CP3002-HDD module.

The board supports one 32-bit/33 MHz CompactPCI interface. When installed in the system slot, the interface is enabled, and when installed in a peripheral slot, the CP3002 is isolated from the CompactPCI bus.

The CP3002 further provides safety and security features via a Trusted Platform Module (TPM) 1.2 on request.

Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments, including I/O intensive applications where only one slot is available for the CPU, making it a perfect core technology for long-life applications. Components which have high temperature tolerance have been selected from embedded technology programs, and therefore offer long-term availability.

There are various operating systems available for the CP3002. For detailed information, please contact Kontron.

1.2 Board-Specific Information

The CP3002 is a CompactPCI single-board computer based on the Intel® Core™ i7 and the Intel® Celeron processor and specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP3002's outstanding features are:

- Support for the following multi-chip package (MCP) processors:
  - Intel® Core™ i7-610E (SV), 2.53 GHz, 4 MB L3 cache
  - Intel® Core™ i7-620LE (LV), 2.0 GHz, 4 MB L3 cache
  - Intel® Core™ i7-660UE (ULV), 1.33 GHz, 4 MB L3 cache
  - Intel® Celeron® U3405 (ULV), 1.07 GHz, 2 MB L3 cache
- Intel® QM57 Express chipset
- Up to 8 GB, dual-channel, DDR3 SDRAM memory with ECC running at 1066 MHz
- Integrated 3D high-performance graphics controller
- VGA display support for up to QXGA (2048 x 1536 pixels) resolution
- Two Gigabit Ethernet controllers with Wake-on-LAN support (Intel® 82574L), switchable to rear I/O
- Six Serial ATA (SATA) interfaces with SATA RAID 0/1/5/10 support:
  - One SATA interface for the standard SATA onboard connector
  - One SATA interface for the Serial ATA Flash module (SSD)
  - Two SATA interfaces for the high-speed I/O extension connector
  - Two SATA interfaces for rear I/O
- Six USB ports:
  - Two USB 2.0 on front I/O
  - Two USB 2.0 on rear I/O
  - Two USB 2.0 interfaces for the onboard high-speed I/O extension connector
- 32-bit, 33 MHz PCI CompactPCI interface for support of up to seven peripheral slots (7x REQ/GNT signals)
- Compatible with CompactPCI Specification PICMG 2.0 Rev. 3.0 and usable in the system controller slot as well as in a peripheral slot (the PCI interface is isolated in peripheral slot)
- TCG 1.2 compliant Trusted Platform Module (TPM), on request
- Two SPI boot flashes for two separate uEFI BIOS images:
  - One standard SPI boot flash
  - One recovery SPI boot flash
- Watchdog timer
- Battery-backed real-time clock (RTC)
- Two COM ports:
  - COMA either on the 8HP expansion module or on the rear I/O
  - COMB on the rear I/O
- Peripheral extension connectors:
  - High-speed I/O extension connector
  - SPI extension connector
- Rear I/O on the CompactPCI connector J2
- 4HP or 8HP, 3U CompactPCI
- Several rear I/O configurations
- Power-up sequencing and in-rush current optimized design
- Passive heat sink solution for forced airflow cooling
- AMI Aptio®, a uEFI-compliant platform firmware

1.3 System Expansion Capabilities

1.3.1 CP3002-HDD Module

The CP3002-HDD module for the 8HP CP3002 version provides legacy PC I/O ports. It includes one digital DVI port, two USB 2.0 ports, one COM port, and one CFast card socket. A SATA hard disk interface is also available for installing a Serial ATA 2.5” HDD or SSD. The CP3002-HDD module cannot be used in conjunction with the SATA Flash module.

For further information concerning the CP3002-HDD module, refer to Appendix A.

1.3.2 CP-RIO3-04 Rear I/O Module

The CP-RIO3-04 rear I/O module has been designed for use with the CP3002 board from Kontron and provides comprehensive rear I/O functionality.

For further information concerning the CP-RIO3-04 rear I/O module, refer to Appendix B.

1.3.3 Serial ATA Flash Module

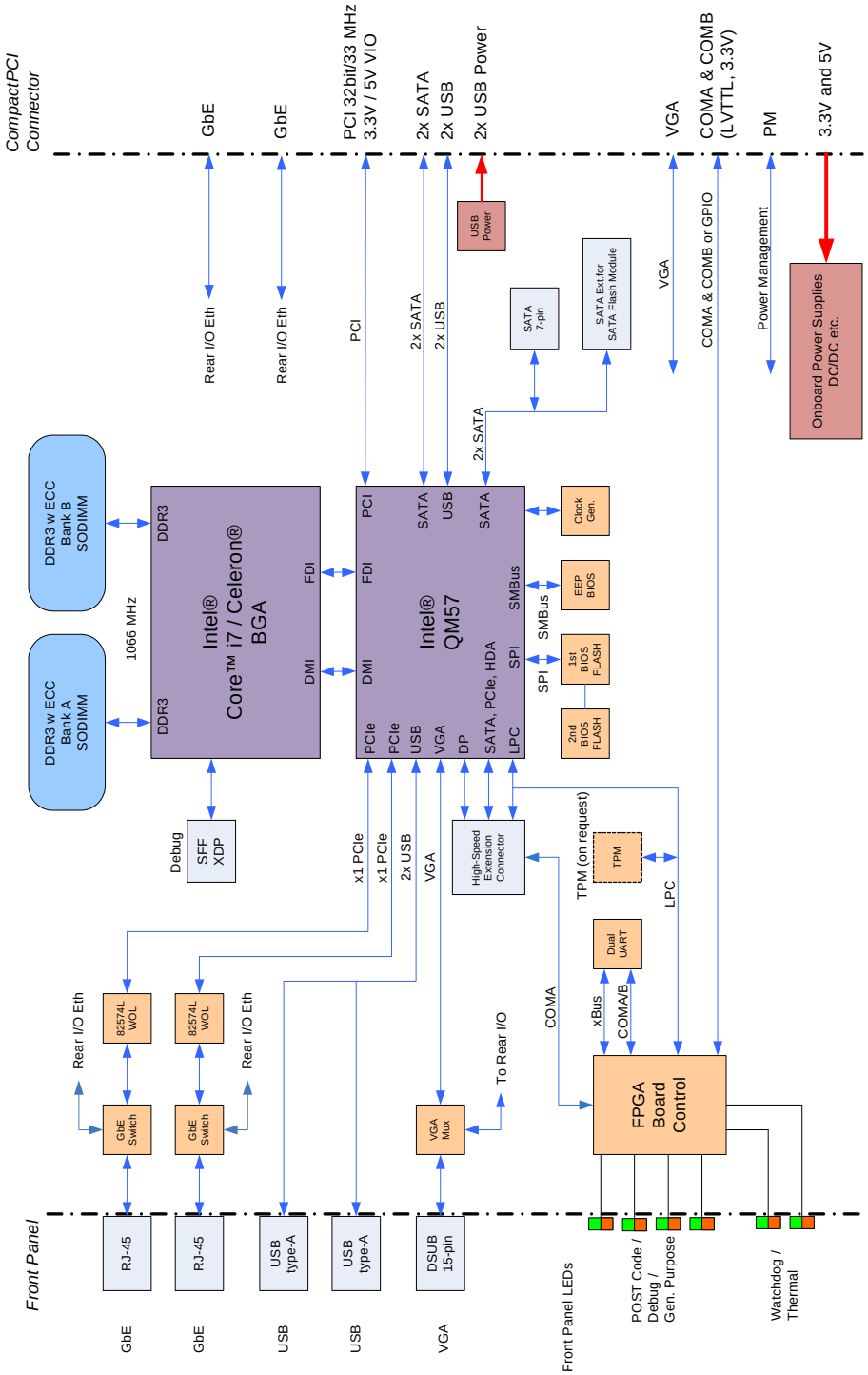
The 4HP CP3002 provides support for up to 16 GB of Serial ATA flash memory in combination with an optional Serial ATA Flash module, which is connected to an onboard connector. For further information concerning the Serial ATA Flash module, refer to Appendix C.

1.4 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

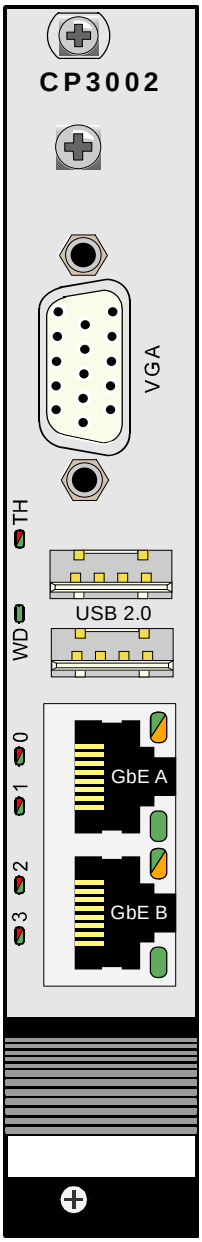
1.4.1 Functional Block Diagram

Figure 1-1: CP3002 Functional Block Diagram



1.4.2 Front Panel

Figure 1-2: 4HP CP3002 Front Panel



LEGEND:

Watchdog and Overtemperature Status LEDs:

WD (green):	Watchdog Status
TH (red/green):	Overtemperature Status

General Purpose LEDs:

LED0..3 (red/green/red+green):	General Purpose/POST Code

Note ...

If the General Purpose LEDs 0..3 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started.

For further information, please contact Kontron.

Ethernet LEDs:

ACT (green):	Ethernet Link/Activity
SPEED (green/orange):	Ethernet Speed

Note ...

For information regarding the front panel of the 8HP CP3002, refer to Appendix A, CP3002-HDD Module.

1.4.3 Board Layout

Figure 1-3: 4HP CP3002 Board Layout (Top View)

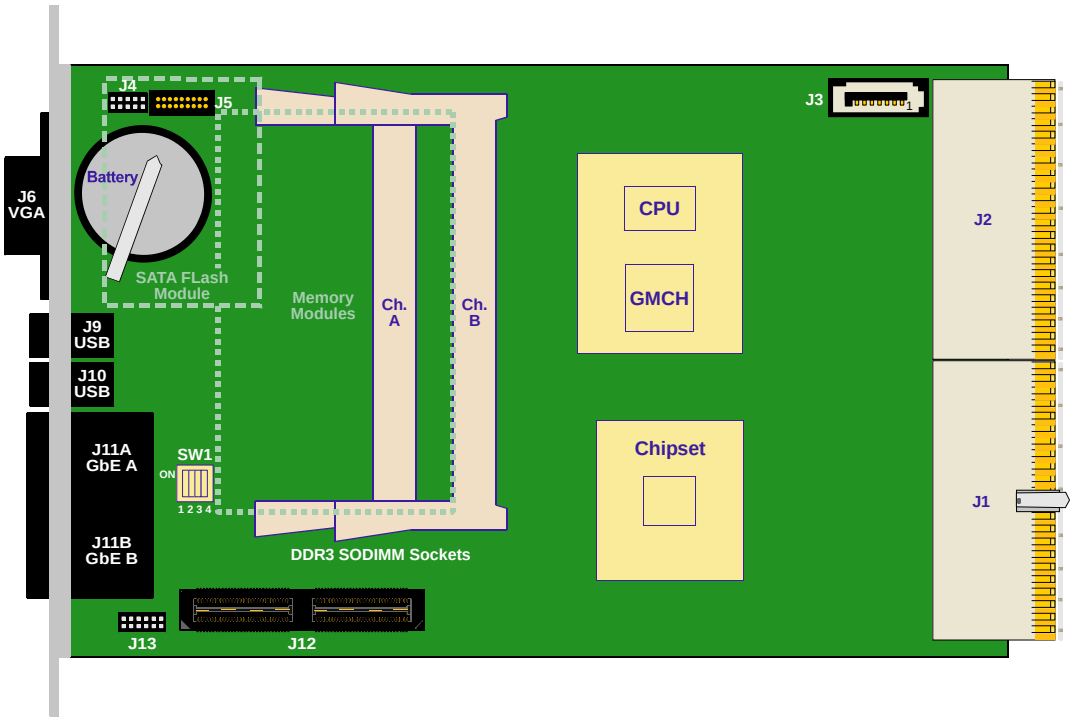
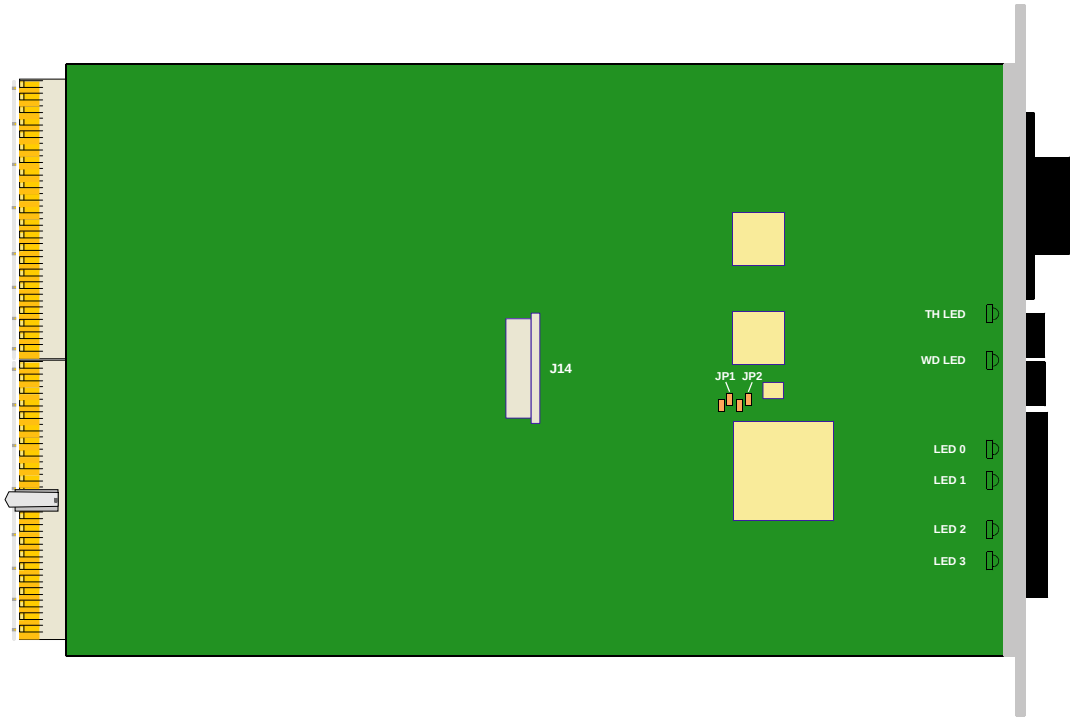


Figure 1-4: 4HP CP3002 Board Layout (Bottom View)



1.5 Technical Specification

Table 1-1: CP3002 Main Specifications

FEATURES		SPECIFICATIONS
Processor and Memory	CPU	The CP3002 supports the following microprocessors: • Intel® Core™ i7-610E (SV), 2.53 GHz, 4 MB L3 cache • Intel® Core™ i7-620LE (LV), 2.0 GHz, 4 MB L3 cache • Intel® Core™ i7-660UE (ULV), 1.33 GHz, 4 MB L3 cache • Intel® Celeron® U3405 (ULV), 1.07 GHz, 2 MB L3 cache Further processor features: • Two execution cores • Intel® Hyper-Threading Technology (Core™ i7) • Intel® 64 Architecture • Intel® Turbo Boost Technology (Core™ i7) • Intel® Intelligent Power Sharing (Core™ i7) • System Memory interface with optimized support for dual-channel DDR3 SDRAM memory at 1066 MHz with ECC • Integrated 2D and 3D Graphics Engines • DMI and FDI interfaces to the Intel® QM57 chipset • Two x8 PCI Express 2.0 ports operating at 2.5 GT/s Please contact Kontron for further information concerning the suitability of other Intel processors for use with the CP3002.

	Memory	Main Memory:
		• Up to 8 GB, dual-channel DDR3 SDRAM memory with ECC running at 1066 MHz on two SODIMM sockets
		Cache Structure:
		• 64 kB L1 cache for each core
		  • 32 kB instruction cache
		  • 32 kB data cache
		• Up to 512 kB L2 shared instruction/data cache for each core
		• Up to 4 MB L3 shared instruction/data cache shared between both cores
		Flash Memory:
		• Two redundant SPI boot flashes (2 x 8 MB) for two separate uEFI BIOS images
		• Up to 16 GB NAND flash via an onboard Serial ATA Flash module (SSD)
		Serial EEPROM with 64 kbit

Table 1-1: CP3002 Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Chipset	Intel® QM57	Mobile Intel® QM57 Express Chipset: • Two x4 or eight x1 PCI Express 2.0 ports operating at 2.5 GT/s (only two x1 PCI Express ports are used) • SATA host controller with six ports, 3 Gbit/s data transfer rate and RAID 0/1/5/10 support • USB 2.0 host interface with up to 14 USB ports available (only six ports are used) • SPI flash interface support • Low Pin Count (LPC) interface • PCI interface, 32-bit/33 MHz • Power management logic support • Enhanced DMA controller, interrupt controller, and timer functions • System Management Bus (SMBus) compatible with most I²C™ devices • DMI and FDI interfaces to the processor • High Definition Audio (HDA) interface (not used) • Analog display port • Three digital display ports (only one port is used) • Integrated RTC
Integrated Controller	Graphics controller	High-performance 3D graphics controller integrated in the processor: • Support for two independent displays • Supports digital display resolutions up to 2560 x 1600 pixels @ 60 Hz • Supports analog display resolutions up to 2048 x 1536 pixels @ 75 Hz • Dynamic Video Memory Technology (DVMT)

Table 1-1: CP3002 Main Specifications (Continued)

	FEATURES	SPECIFICATIONS
Interfaces	CompactPCI	Compliant with CompactPCI Specification PICMG® 2.0 R 3.0: • System master operation • 32-bit/33 MHz master interface • 3.3 V or 5 V (universal PCI interface) • Support for up to seven peripheral slots (7x REQ/GNT signals) When installed in a peripheral slot, the CP3002 is isolated from the CompactPCI bus. It receives power from the backplane and supports rear I/O. CP3002 removal under power: When installed in a peripheral slot, the CP3002 supports hot plugging on the power interface through a dedicated power controller, but not on the PCI interface. Hot swapping of peripheral boards controlled by the CP3002: When installed in the system controller slot, the CP3002 supports the hot swapping of other boards. Individual clocks for each slot and Enum signal handling are in compliance with the PICMG 2.1 Hot Swap Specification. The CP3002 itself, however, is not hot swappable. When installed in the system controller slot, the system must be powered down in order to replace the board.
	Rear I/O	The following interfaces are routed to the rear I/O connector J2: • COMA and COMB (3.3V LVTTL signaling) • 2 x USB 2.0 • VGA (analog) • 2x Gigabit Ethernet • 2x SATA • System management signals • Input for 5V standby power • General purpose signals
	Gigabit Ethernet	Two 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on the Intel® 82574L Ethernet PCI Express bus controller individually switchable to front I/O or rear I/O: • Dual RJ-45 connector on the front panel • Automatic mode recognition (Auto-Negotiation) • Automatic cabling configuration recognition (Auto-MDI/X) • Wake-on-LAN support
	USB	Six USB ports supporting UHCI (USB 1.1) and EHCI (USB 2.0): • Two USB 2.0 ports on the front I/O • Two USB 2.0 ports on the rear I/O interface • Two USB 2.0 interfaces for the onboard high-speed I/O extension connector

Table 1-1: CP3002 Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Interfaces	Serial	Two 16C550-compatible UARTs: • COMA available on the 8HP expansion module or on rear I/O • COMB available on rear I/O only
	Serial ATA	Serial ATA Host Controllers integrated in the Intel® QM57 chipset: • Provide support for six SATA ports, two onboard, two on rear I/O, and two on the 8HP extension module • Data transfer rates up to 300 MB/s • High-performance RAID 0/1/5/10 functionality on all SATA ports
	I/O Expansion Interfaces	I/O expansion to 8HP board version: • 2x SATA • 2x USB2.0 • DP (DisplayPort) • COMA • Monitor and control signals • LPC • HDA • PCI Express
Sockets	Front Panel Connectors	• VGA: 15-pin D-Sub connector • USB: two 4-pin, type A connectors • Ethernet: dual RJ-45 connector
	Onboard Connectors	• 7-pin, L-form standard SATA II connector, J3 • High-speed I/O extension connector, J12 • SPI extension connector, J4 • 18-pin extension connector for SATA Flash module (SSD), J5 • JTAG connector, J13 • XDP-SFF (debug) connector, J14 • CompactPCI Connectors J1 and J2 • Two 204-pin DDR3 SODIMM sockets
LEDs	LEDs	Watchdog and Overtemperature Status LEDs: • WD (green): Watchdog Status • TH (red/green): Overtemperature Status General Purpose LEDs: • LED0..3 (red/green/red+green): General Purpose/POST Code Ethernet LEDs: • ACT (green): Network/Link Activity • SPEED (green/orange): Network Speed

Table 1-1: CP3002 Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Timer	Watchdog Timer	• Software-configurable, two-stage Watchdog with programmable timeout ranging from 125 ms to 4096 s in 16 steps • Serves for generating IRQ or hardware reset
	System Timer	• The Intel® QM57 chipset contains three 8254-style counters which have fixed uses • In addition to the three 8254-style counters, the Intel® QM57 chipset includes eight individual high-precision event timers that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register.

System Management	Thermal Management	CPU and board overtemperature protection is provided by:
		• Temperature sensors integrated in processor:
		  • Two temperature sensors for monitoring the processor cores
		  • One temperature sensor for monitoring the graphics controller and the memory controller
		• One temperature sensor integrated in the Intel® QM57 chipset for monitoring the chipset
		• Specially designed heat sink

Security	TPM	Trusted Platform Module (TPM) 1.2 for enhanced hardware- and software-based data and system security (on request)
Software	uEFI BIOS	AMI Aptio®, AMI's next-generation BIOS firmware based on the uEFI Specification and the Intel Platform Innovation Framework for EFI. • LAN boot capability for diskless systems (standard PXE) • Redundant image; automatic fail-safe recovery in case of a damaged image • Non-volatile storage of setting in the SPI flash (battery only required for the RTC) • Compatibility Support Module (CSM) providing legacy BIOS compatibility based on AMIBIOS8 • Command shell for diagnostics and configuration • EFI shell commands executable from mass storage device in a Pre-OS environment (open interface)
	Operating Systems	There are various operating systems available for the CP3002. For detailed information, please contact Kontron.

Table 1-1: CP3002 Main Specifications (Continued)

	FEATURES	SPECIFICATIONS
General	Mechanical	3U, 4HP, CompactPCI-compliant form factor
	Power Consumption	See Chapter 5 for details.
	Temperature Range	Operational: 0°C to +60°C Standard (depending on processor version and airflow in the system) -25°C to +70°C Extended (depending on processor version and airflow in the system) Storage: -55°C to +85°C Without hard disk and without battery *Note ...* When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP3002 (See "Battery" below). *Note ...* When additional components are installed, refer to their operational specifications as this will influence the operational and storage temperature of the CP3002.
	Battery	3.0V lithium battery for RTC with battery socket. Recommended type: CR2025 Temperature ranges: Operational (load): -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -55°C to +70°C typical (no discharge)
	Climatic Humidity	93% RH at 40 °C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 160 mm
	Board Weight	337 grams (4 HP CP3002 with heat sink, front panel, two 2 GB SODIMM memory modules, and battery but without SATA Flash module)

Note ...

For a description of the additional 8HP version interfaces, refer to Appendix A, CP3002-HDD Module.

1.6 Standards

This product complies with the requirements of the following standards.

Table 1-2: Standards

TYPE	ASPECT	STANDARD
CE	Emission	EN55022 EN61000-6-3
	Immission	EN55024 EN61000-6-2
	Electrical Safety	EN60950-1
Mechanical	Mechanical Dimensions	IEEE 1101.10
Environmental	Climatic Humidity	IEC60068-2-78 (see note below)
	WEEE	Directive 2002/96/EC Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC Restriction of the use of certain hazardous substances in electrical and electronic equipment

Note ...

Kontron performs comprehensive environmental testing of its products in accordance with applicable standards.

Customers desiring to perform further environmental testing of Kontron products must contact Kontron for assistance prior to performing any such testing. This is necessary, as it is possible that environmental testing can be destructive when not performed in accordance with the applicable specifications.

In particular, for example, boards **without conformal coating** must not be exposed to a change of temperature exceeding 1K/minute, averaged over a period of not more than five minutes. Otherwise, condensation may cause irreversible damage, especially when the board is powered up again.

Kontron does not accept any responsibility for damage to products resulting from destructive environmental testing.

In addition, boards ordered with the ruggedized service comply with the following standards as well.

Table 1-3: Additional Standards for Boards Ordered with Ruggedized Service

TYPE	ASPECT	STANDARD	REMARKS
Environmental	Vibration (Sinusoidal)	IEC60068-2-6	Ruggedized version test parameters: • 10-300 (Hz) frequency range • 5 (g) acceleration • 1 (oct/min) sweep rate • 10 cycles/axis • 3 axis
	Single Shock	IEC60068-2-27	Ruggedized version test parameters: • 30 (g) acceleration • 9 (ms) shock duration half sine • 3 number of shocks per direction (total: 18) • 6 directions • 5 (s) recovery time
	Permanent Shock	IEC60068-2-29	Ruggedized version test parameters: • 15 (g) acceleration • 11 (ms) shock duration half sine • 500 number of shocks per direction • 6 directions • 5 (s) recovery time

Furthermore, boards providing ruggedized service and conformal coating comply with the following standards as well.

Table 1-4: Add. Standards for CP3002 with Rug. Service and Conformal Coating

TYPE	ASPECT	STANDARD	REMARKS
Environmental	Random Vibration (Broadband)	VITA 47, Class V1	Test parameters: 5-100 (Hz) frequency range 0.04 (g^2/Hz) acceleration 60 min//axis test duration 3 axes
	Single Shock	VITA 47, Class OS1	Test parameters: 20 (g) acceleration 11 (ms) half-sine shock duration 3 number of shocks per direction (total: 18) 6 directions 5 (s) recovery time
	Temperature	VITA 47, Class AC3	Test parameters: -20°C to +70°C operating temperature forced airflow 3 m/s Above +65°C, the CPU performance may be reduced, depending on application demands and system cooling capabilities.
		VITA 47, Class C4	Test parameters: -55°C to +105°C storage temperature
	Climatic Humidity	VITA 47	Test parameters: 30°C to 60°C, 10*24h cyclic temperature 95% RH

Note ...

When additional modules are used with a ruggedized and coated CP3002, please refer to the specifications of the respective module as this may have an impact on the environmental conditions of the board.

1.7 Related Publications

The following publications contain information relating to this product.

Table 1-5: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems	CompactPCI Specification PICMG 2.0, Rev. 3.0 CompactPCI Hot Swap Specification PICMG 2.1 Rev. 2.0
Serial ATA	Serial ATA 1.0a Specification
CFast	CFast Specification Revision 1.0
Platform Firmware	Unified Extensible Firmware Interface (uEFI) specification, version 2.1
All Kontron products	Product Safety and Implementation Guide, ID 1021-9142

Chapter 2

Functional Description

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2. Functional Description

2.1 Processor

The board supports the Intel® Core™ i7-610E processor with 2.53 GHz clock speed, the Intel® Core™ i7-620LE processor with 2.0 GHz clock speed, the Intel® Core™ i7-660UE processor with 1.33 GHz clock speed, and the Intel® Celeron® U3405 processor with 1.07 GHz clock speed.

The processor used on the CP3002 includes an integrated high-performance graphics controller and a DDR3 dual-channel memory controller with ECC support as well as one x16 PCI Express 2.0 port operating at 2.5 GT/s. They support various technologies, such as:

- Intel® Hyper-Threading Technology (Core™ i7)
- Intel® Turbo Boost Technology (Core™ i7)
- Intel® Intelligent Power Sharing (Core™ i7)
- Intel® SpeedStep® Technology
- Intel® Virtualization Technology
- Intel® Streaming SIMD Extensions 4.1
- Intel® Streaming SIMD Extensions 4.2
- Intel® 64 Architecture
- Execute Disable Bit

The Intel® Hyper-Threading Technology allows one execution core to function as two logical processors. When this feature is enabled in the uEFI BIOS, four processor cores are present to the operating system. This results in higher processing throughput and improved performance on the multithreaded software.

The Intel® Turbo Boost Technology and the Intel® Intelligent Power Sharing technology allow the processor and the graphics controller to opportunistically and automatically run faster than its rated operating clock frequency if it is operating below power, temperature, and current limits.

The Intel® SpeedStep® technology enables real-time dynamic switching of the voltage and frequency between several modes. This is achieved by switching the bus ratios, the core operating voltage, and the core processor speeds without resetting the system.

The Intel® Core™ i7 processors used with the CP3002 have the following multi-level cache structure:

- 64 kB L1 cache for each core
  - 32 kB instruction cache
  - 32 kB data cache
- 256 kB L2 instruction/data cache for each core
- 4 MB L3 shared instruction/data cache shared between both cores

The Intel® Celeron® processor used with the CP3002 has the following multi-level cache structure:

- 64 kB L1 cache for each core
  - 32 kB instruction cache
  - 32 kB data cache
- 512 kB L2 instruction/data cache for each core
- 2 MB L3 shared instruction/data cache shared between both cores

Table 2-1: Features of the Processors Supported on the CP3002

FEATURE	Core™ i7-610E (SV) 2.53 GHz	Core™ i7-620LE (LV) 2.0 GHz	Core™ i7-660UE (ULV) 1.33GHz	Celeron® U3405 (ULV) 1.07 GHz
High Frequency Mode (HFM)	2.53 GHz	2.0 GHz	1.33 GHz	1.07 GHz
Low Frequency Mode (LFM)	1.2 GHz	1.2 GHz	666 MHz	666 MHz
Maximum Turbo Frequency	3.2 GHz	2.8 GHz	2.4 GHz	--
L1 cache per core	64 kB	64 kB	64 kB	64 kB
L2 cache per core	256 kB	256 kB	256 kB	512 kB
L3 cache	4 MB	4 MB	4 MB	2 MB
DDR3 Memory	up to 8 GB / 1066 MHz	up to 8 GB / 1066 MHz	up to 8 GB / 1066 MHz	up to 8 GB / 1066 MHz
Graphics Base Frequency	500 MHz	266 MHz	166 MHz	166 MHz
Graphics Max. Dynamic Frequency	766 MHz	566 MHz	500 MHz	500 MHz
Thermal Design Power	35 W	25 W	18 W	18 W
Package	BGA (1288)	BGA (1288)	BGA (1288)	BGA (1288)

2.2 Memory

The CP3002 supports a dual-channel (72-bit) DDR3 memory with Error Checking and Correcting (ECC) running at 1066 MHz. It provides two 204-pin sockets for two DDR3 ECC SODIMM modules that support up to 8 GB system memory. The maximum memory size per channel is 4 GB. The available memory module configuration can be either 2 GB, 4 GB or 8 GB. However, when the internal graphics controller is enabled, the amount of memory available to applications is less than the total physical memory in the system. For example, the chipset's Dynamic Video Memory Technology dynamically allocates the proper amount of system memory required by the operating system and the application.

Table 2-2: Supported Memory Configurations

CHANNEL A (SODIMM)	CHANNEL B (SODIMM)	TOTAL PHYSICAL MEMORY	TOTAL MEMORY AVAILABLE TO APPLICATIONS
2 GB	--	2 GB	2 GB minus the allocated memory for DVMT
--	2 GB	2 GB	2 GB minus the allocated memory for DVMT
2 GB	2 GB	4 GB	4 GB minus the allocated memory for DVMT
4 GB	--	4 GB	4 GB minus the allocated memory for DVMT
--	4 GB	4 GB	4 GB minus the allocated memory for DVMT
4 GB	4 GB	8 GB	8 GB minus the allocated memory for DVMT

Note ...

When the CP3002 is populated with 4 GB or 8 GB physical memory and used with a 32-bit operating system, the CP3002 provides even less memory to applications than indicated in the table above. In this event, the total memory available to the applications depends on the system configuration.

Note ...

Only qualified DDR3 ECC SODIMM modules from Kontron are authorized for use with the CP3002. Replacement of the SODIMM modules by the customer without authorization from Kontron will void the warranty.

Note ...

To achieve full memory performance, it is recommended to populate both memory channels.

2.3 Intel® QM57 Express Chipset

The CP3002 is equipped with the mobile Intel® QM57 Express Chipset, a highly integrated platform controller hub (PCH) with the following features:

- Two x4 or eight x1 PCI Express 2.0 ports operating at 2.5 GT/s (only two x1 PCI Express ports are used)
- SATA host controller with six ports, 3 Gbit/s data transfer rate and RAID 0/1/5/10 support
- USB 2.0 host interface with up to 14 USB 2.0 ports available (only six ports are used)
- SPI interface support
- Low Pin Count (LPC) interface
- PCI interface, 32-bit/33 MHz
- Power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions
- System Management Bus (SMBus)
- DMI and FDI interfaces to the processor
- Intel® High Definition Audio Interface (not used)
- Analog display port
- Three digital display ports (only one port is used)
- Integrated RTC

2.4 Timer

The CP3002 is equipped with the following timers:

- Real-Time Clock
  The Intel® QM57 chipset integrates an MC146818B-compatible real-time clock with 256 Byte CMOS RAM. All CMOS RAM data remain stored in an additional EEPROM device to prevent data loss.
- Counter/Timer
  Three 8254-style counter/timers are included on the CP3002 as defined for the PC/AT.
- The Intel® QM57 chipset integrates eight high-precision event timers.

2.5 Watchdog Timer

The CP3002 provides a Watchdog timer that is programmable for a timeout period ranging from 125 ms to 4096 s in 16 steps. Failure to trigger the Watchdog timer in time results in a system reset or an interrupt. In dual-stage mode, a combination of both interrupt and reset if the Watchdog is not serviced. A hardware status flag will be provided to determine if the Watchdog timer generated the reset.

2.6 Battery

The CP3002 is provided with a 3.0 V “coin cell” lithium battery for the RTC. For further information concerning the battery and its replacement, refer to Chapter 3.5.7, Battery Replacement.

Note ...

If an 8HP expansion module is used on the CP3002, either the CP3002 or the expansion module may be equipped with a battery.

Using one battery on the CP3002 and one on the expansion module simultaneously may result in premature discharge of the batteries.

2.7 Reset

The CP3002 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.7 V for the 5 V line and below 3.1 V for the 3.3 V line, or in the event of a power failure of the DC/DC converters. Other reset sources include the Watchdog timer and the push-button switch on the 8HP front panel. The CP3002 responds to any of these sources by initializing local peripherals.

A reset will be generated if one the following events occurs:

- +5 V supply falls below 4.7 V typical; level-sensitive
- +3.3 V supply falls below 3.1 V typical; level-sensitive
- Power failure of at least one onboard DC/DC converter; level-sensitive
- Push-button "RESET" pressed (only on CP3002-HDD); edge-sensitive
- Watchdog expired; edge-sensitive
- CompactPCI backplane PRST# input (CompactPCI connector J2, pin C17); edge-sensitive
- CompactPCI backplane RST# input (software configurable when the board is in peripheral mode); edge-sensitive

2.8 Flash Memory

The CP3002 provides flash interfaces for redundant uEFI BIOS and the SATA Flash module.

2.8.1 SPI Boot Flash for uEFI BIOS

The CP3002 provides two SPI boot flash chips (2 x 8 MB) for two separate uEFI BIOS images, a standard SPI boot flash and a recovery SPI boot flash. The configuration for the uEFI BIOS recovery can be controlled via the DIP switch SW1, switch 2.

The SPI boot flash includes a hardware write protection option, which can be configured via the uEFI BIOS. If write protection is enabled, the SPI boot flash cannot be written to.

The SPI boot flash includes a hardware write protection option, which can be configured via the uEFI BIOS. If write protection is enabled, the SPI boot flash cannot be written to.

Note ...

The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash.Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

2.8.2 Serial ATA Flash Module (Optional)

The 4HP CP3002 supports up to 16 GB of Serial ATA flash memory in combination with an optional Serial ATA Flash module, which is connected to the onboard connector J5. The SATA Flash module cannot be used in conjunction with the CP3002-HDD module.

The Serial ATA Flash module is an SLC-based SATA NAND flash drive with a built-in full hard-disk emulation and a high data transfer rate (sustained read rate with up to 50 MB/s and sustained write rate with up to 45 MB/s). It is optimized for embedded systems providing high performance, reliability and security.

Note ...

Write protection is available for the SATA Flash module. Please contact Kontron for further assistance if write protection is required.

2.9 8HP Expansion Module

The CP3002 supports the CP3002-HDD as an optional 8HP expansion module via the 120-pin high-speed I/O extension connector J12. This module cannot be used in conjunction with the SATA Flash module. For further information regarding the CP3002-HDD module, refer to Appendix A.

2.10 Trusted Platform Module 1.2 (On Request)

The CP3002 has been designed to support the Trusted Platform Module (TPM) 1.2. This feature is available on request. TPM1.2 is a security chip specifically designed to provide enhanced hardware- and software-based data and system security. It stores sensitive data such as encryption and signature keys, certificates and passwords, and is able to withstand software attacks to protect the stored information.

Hardware features of the TPM 1.2:

- TCG 1.2 compliant Trusted Platform Module (TPM)
- Security architecture based on the Infineon SLE66CXxxPE security controller family
- EEPROM for TCG firmware enhancements and for user data and keys
- Advanced Crypto Engine (ACE) with RSA support up to 2048-bit key length
- Hardware accelerator for SHA-1 hash algorithm
- True Random Number Generator (TRNG)
- Tick counter with tamper detection
- Protection against Dictionary Attack
- Intel® Trusted Execution Technology Support
- Full personalization with Endorsement Key (EK) and EK certificate

2.11 Board Interfaces

2.11.1 Front Panel LEDs

The CP3002 is equipped with one Watchdog Status LED (WD LED), one Temperature Status LED (TH LED), and four General Purpose/POST code LEDs (LED0..3). Their functionality is described in the following chapters and reflected in the registers mentioned in Chapter 4, Configuration.

2.11.1.1 Watchdog and Temperature Status LEDs

The CP3002 provides one Watchdog Status LED (WD LED) and one Temperature Status LED (TH LED).

Table 2-3: Watchdog and Thermal Status LEDs

LED	COLOR	FUNCTION AFTER BOOT-UP
WD LED	green	Watchdog status: off = Watchdog inactive (default) on = Watchdog active, waiting to be triggered
TH LED	red	Processor overtemperature: on = processor temperature is above the safe operating area blinking = processor has reached a junction temperature of approximately 125°C (Thermtrip)
	green	The processor is in a safe operating area.

Note ...

If the TH LED flashes red on and off at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Once activated, the Thermtrip event remains latched until a cold restart of the CP3002 is undertaken (all power off and then on again).

2.11.1.2 General Purpose LEDs

The CP3002 provides four General Purpose LEDs (LED0..3) on the front panel. They are designed to indicate the boot-up POST code after which they are available to the application.

If the LED0..3 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started. In this case, check the power supply. If the power supply appears to be functional and the LEDs are still red, please contact Kontron.

The POST code is indicated during the boot-up phase. After boot-up, the LEDs indicate General Purpose or Port 80 signals, depending on the uEFI BIOS settings. The default setting after boot-up is General Purpose.

Table 2-4: General Purpose LED Function

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION DURING uEFI BIOS POST (if POST code config. is enabled)	FUNCTION AFTER BOOT-UP
LED3	red	When lit up during boot-up, it indicates a power failure.	--	General Purpose or Port 80 *Default: General Purpose*
	green	--	uEFI BIOS POST bit 3 and bit 7	
	red+green	--	--	
LED2	red	When lit up during boot-up, it indicates a CPU catastrophic error.	--	General Purpose or Port 80 *Default: General Purpose*
	green	--	uEFI BIOS POST bit 2 and bit 6	
	red+green	--	--	
LED1	red	When lit up during boot-up, it indicates a hardware reset.	--	General Purpose or Port 80 *Default: General Purpose*
	green	--	uEFI BIOS POST bit 1 and bit 5	
	red+green	--	--	
LED0	red	When lit up during boot-up, it indicates a uEFI BIOS boot failure.	--	General Purpose or Port 80 *Default: General Purpose*
	green	--	uEFI BIOS POST bit 0 and bit 4	
	red+green	--	--	

For further information regarding the configuration of the General Purpose LEDs, refer to Chapter 4.3.14, LED Configuration Register, and Chapter 4.3.15, LED Control Register.

Note ...

The bit allocation for Port 80 is the same as for the POST code.

How to Read the 8-Bit POST Code

Due to the fact that only 4 bits are available and 8 bits must be displayed, the POST code output is multiplexed on the General Purpose LEDs.

Table 2-5: POST Code Sequence

STATE	GENERAL PURPOSE LEDs
0	All LEDs are OFF; start of POST sequence
1	High nibble
2	Low nibble; state 2 is followed by state 0

The following is an example of the General Purpose LEDs' operation if the POST configuration is enabled (see also Table 2-4, "General Purpose LED Function").

Table 2-6: POST Code Example

	LED3	LED2	LED1	LED0	RESULT
HIGH NIBBLE	off (0)	on (1)	off (0)	off (0)	0x4
LOW NIBBLE	off (0)	off (0)	off (0)	on (1)	0x1
POST CODE					0x41

Note ...

Under normal operating conditions, the General Purpose LEDs should not remain lit during boot-up. They are intended to be used only for debugging purposes. In the event that a General Purpose LED lights up during boot-up and the CP3002 does not boot, please contact Kontron for further assistance.

2.11.2 DIP Switch SW1

The CP3002 is equipped with one 4-bit DIP switch, SW1, used for board configuration.

Table 2-7: DIP Switch SW1 Function

SWITCH	FUNCTION
1	POST code indication on LED0..3
2	SPI flash boot configuration
3	Reset configuration
4	Clear uEFI BIOS settings

2.11.3 USB Interfaces

The CP3002 supports six USB 2.0 ports: two on front I/O, two on the high-speed I/O extension connector J12, two on the rear I/O CompactPCI connector J2. All six ports are high-speed, full-speed, and low-speed capable.

One USB peripheral may be connected to each port. For connecting more USB devices to the CP3002 than there are available ports, an external USB hub is required.

Note ...

When connecting peripheral devices to USB2.0 ports, always ensure that appropriate cables are used.

2.11.3.1 Front Panel USB Connectors J9 and J10

The CP3002 has two USB 2.0 interfaces that are implemented as two 4-pin, type A USB connectors on the front panel, J9 and J10, with the following pinout:

Figure 2-1: USB Connectors J9 and J10

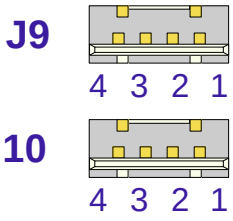


Table 2-8: USB Connectors J9 and J10 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	O
2	USB-	Differential USB-	I/O
3	USB+	Differential USB+	I/O
4	GND	GND	--

Note ...

The CP3002 host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

2.11.4 Integrated Graphics Controller

The processor includes a highly integrated graphics accelerator delivering high performance 3D, 2D graphics capabilities. The integrated graphics controller has two independent display pipes allowing for support of two independent display screens.

Integrated 2D/3D graphics:

- Intel® Dynamic Video Memory Technology
- Intel® Graphics Performance Modulation Technology
- Intel® Smart 2D Display Technology
- High-performance MPEG-2 decoding
- WMV9/VC1 Hardware acceleration
- Support of DisplayPort interface
- Analog display support for resolution up to 2048 x 1536 pixels @ 75 Hz
- Digital display support for resolution up to 2560 x 1600 pixels @ 60 Hz

2.11.4.1 Graphics Memory Usage

The processor supports the Dynamic Video Memory Technology (Intel® DVMT) with up to 352 MB memory. This technology ensures the most efficient use of all available memory for maximum 3D graphics performance. DVMT dynamically responds to application requirements allocating display and texturing memory resources as required.

2.11.4.2 VGA Analog Interface and Connector J6

The 15-pin female connector J6 is used to connect a VGA analog monitor to the CP3002.

Figure 2-2: D-Sub VGA Con. J6

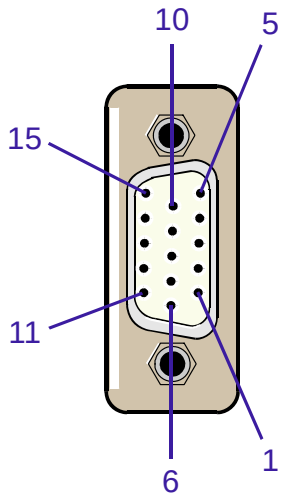


Table 2-9: D-Sub VGA Connector J6 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	Red	Red video signal output	O
2	Green	Green video signal output	O
3	Blue	Blue video signal output	O
10*	VGA_DETECT	Monitor detection signal	I
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I^2C data	I/O
15	Sclk	I^2C clock	I/O
9	VCC	Power +5V, 1.5 A fuse protection	O
5,6,7,8	GND	Ground signal	--
4,11	NC	--	--

* Pin 10 is normally defined as Ground but is used on the CP3002 as detection signal of a connected monitor if the uEFI BIOS setting for the CP3002 is “AUTO” (the uEFI BIOS default setting is “FRONT”).

Note ...

If the automatic VGA detection mechanism on the CP3002 is used, the user must ensure that the VGA cable and the connected monitor have a GND signal on pin 10. Otherwise the interface is not operable.

Note ...

The VGA interface can be used either on the front panel or on the rear I/O. The VGA signals are switched to front or rear I/O, depending on the uEFI BIOS setting.

2.11.5 Serial Ports

The CP3002 provides two serial ports, COMA (3.3V LVTTL) available either on the 8HP version or on the rear I/O, and COMB (3.3V LVTTL) available on the rear I/O.

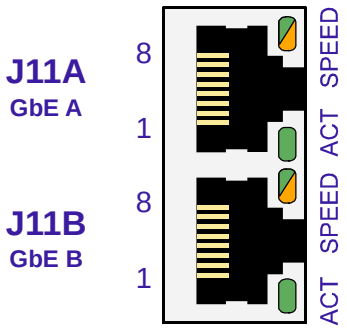
COMA and COMB are fully compatible with the 16C550 controller and include a complete set of handshaking and modem control signals. The COMA and COMB ports provide maskable interrupt generation. The data transfer on the COM ports is up to 115.2 kbit/s.

2.11.6 Gigabit Ethernet

The CP3002 board includes two 10Base-T/100Base-TX/1000Base-T Ethernet ports based on two Intel® 82574L Gigabit Ethernet controllers, which are connected to the x1 PCI Express interfaces of the QM57 chipset.

The Intel® 82574L Gigabit Ethernet Controller's architecture is optimized to deliver high performance with the lowest power consumption. The controller's architecture includes independent transmit and receive queues and a PCI Express interface that maximizes the use of bursts for efficient bus usage.

Figure 2-3: Dual Gigabit Ethernet Connector J11A/B



The Boot-from-LAN and Wake-on-LAN features are supported. Wake-on-LAN is available on all Ethernet interfaces. After an operating system shutdown, a 1000Base-T Gigabit connection is automatically reduced to 100 Mbit or 10 Mbit operation and the Ethernet controller waits to receive a broadcast or unicast packet with an explicit data pattern to assert a signal or a PME message to wake up the system. If the main power is switched off after an OS shutdown, a 5V standby supply must be provided over the J2 rear I/O CompactPCI connector to continue powering the Wake-on-LAN relevant devices.

Note ...

The Ethernet transmission can operate effectively using a CAT5 cable with a maximum length of 100 m.

The Ethernet connectors are realized as RJ-45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

RJ-45 Connector J11A/B Pinout

The J11A/B connector supplies the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller.

Table 2-10: Dual Gigabit Ethernet Connector J11A/B Pinout

PIN	MDI / STANDARD ETHERNET CABLE					
	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-

Ethernet LED Status

ACT (green): This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

SPEED (green/orange): This LED lights up to indicate a successful 100Base-TX or 1000BASE-T connection. When green it indicates a 100Base-TX connection and when orange it indicates a 1000Base-T connection. When not lit and the ACT-LED is active, the connection is operating at 10Base-T.

2.11.7 Serial ATA Interfaces

The CP3002 provides six SATA I (1.5 Gbit/sec) and SATA II (3.0 Gbit/sec) compliant interfaces with RAID support (0/1/5/10), one for the SATA Flash module, one for the onboard SATA connector J3, two for the 8 HP extension module and two for rear I/O. For further information on the SATA Flash Module, refer to Appendix C.

2.11.7.1 Serial ATA Connector J3

The CP3002 is equipped with one standard SATA connector, J3, which is used to connect a standard HDD/SSD or another SATA device to the CP3002.

Figure 2-4: SATA Con. J3

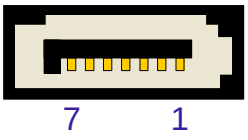


Table 2-11: SATA Connector J3 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	GND	Ground signal	--
2	SATA_TX+	Differential Transmit +	O
3	SATA_TX-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX-	Differential Receive -	I
6	SATA_RX+	Differential Receive +	I
7	GND	Ground signal	--

Note ...

If the onboard SATA connector will be used, due to the big SATA connector and the stiff SATA cable, the CP3002 will exceed the thickness of 4HP.

Note ...

To ensure secure connectivity, the SATA connector supports the use of SATA II cables (SATA cables with locking latch).

2.11.8 Debug Interface

The CP3002 provides several onboard options for hardware and software debugging, such as:

- Four bicolor general purpose LEDs (LED0..3), which indicate hardware failures, uEFI BIOS POST codes and user-configurable outputs
- One JTAG connector, J13, for programming the onboard logic
- One XDP-SFF, processor JTAG connector, J14, for facilitating the debug and uEFI BIOS software development

2.11.9 CompactPCI Interface

The CP3002 supports a flexible CompactPCI interface with a hot plug power interface (no PCI hot swap). In the system controller slot the PCI interface is in transparent mode, and in the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as "passive mode".

2.11.9.1 Board Functionality when Installed in System Controller Slot

In a system controller slot, the CompactPCI interface is provided as 32-bit/33 MHz PCI interface.

The CP3002 supports up to seven peripheral slots through a CompactPCI backplane.

Note ...

The CP3002 supports universal PCI V(I/O) signaling voltages with one common resistor configuration. For both 5V and 3.3 V PCI signaling voltages, 2.7 kΩ pull-up resistors are used.

2.11.9.2 Board Functionality when Installed in Peripheral Slot (Passive Mode)

In a peripheral slot, the board receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated.

2.11.9.3 Front/Rear I/O Configuration

The CP3002 is available in two versions:

- CP3002 front I/O version
- CP3002 rear I/O version

Please ensure that the correct version is stated on the order. If the CP3002 is ordered with rear I/O configuration, various I/O interfaces and signals are available via the CompactPCI connector J2, such as USB, SATA, GbE, VGA, and COM, as well as power and management signals. If the CP3002 is ordered with front I/O configuration, the I/O interfaces and signals mentioned above are isolated from the CompactPCI connector J2.

Note ...

The CP3002 with front I/O configuration does not provide a 64-bit termination to the backplane via the CompactPCI connector J2. This is different than on previous boards such as CP307 or CP308 where 64-bit termination is provided.

2.11.9.4 Board Insertion/Replacement under Power

The following features are implemented on the CP3002:

- Power ramping
- ENUM signal handling (hot swapping of peripheral boards)

Power ramping on the CP3002 provides the hot plug functionality on the power interface. The PCI signal interface does not provide hot swap functionality. No microswitch, no blue LED and no signal precharge are provided on the CP3002.

The ENUM signal on the CP3002 allows for hot swapping of peripheral boards with hot swap capability when the CP3002 is installed in the system controller slot.

Note ...

The CP3002 itself is not hot swappable when inserted in a system controller slot. When inserted in a peripheral slot, the CP3002 is hot pluggable.

2.11.9.5 Power Ramping

On the CP3002 a special power controller is used to ramp up the onboard supply voltages. This is done to avoid transients on the +3.3V and +5V power supplies from the system. When the power supply is stable, the power controller generates an onboard reset to put the board into a defined state.

2.11.9.6 ENUM# Interrupt

If the board is operated in the system controller slot, the ENUM signal is an input.

2.11.10 CompactPCI Connectors J1 and J2

The CP3002 provides two CompactPCI connectors, J1 and J2, with the following functionality:

- J1: 32-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J2: arbitration, clock and optionally rear I/O interface functionality

The CP3002 is designed for a CompactPCI bus architecture and the board is capable of driving up to seven CompactPCI slots with individual arbitration and clock signals.

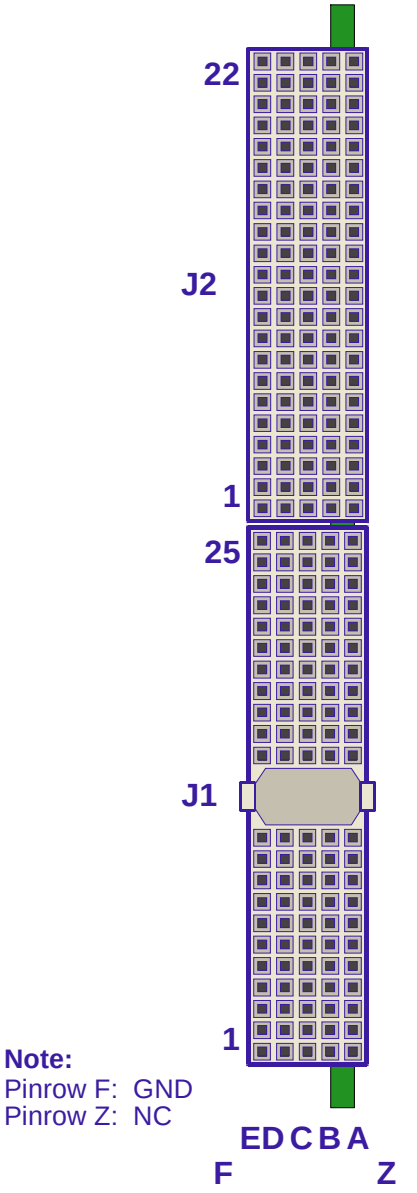
The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.11.10.1 CompactPCI Connector Keying

CompactPCI backplane connectors support guide lugs to ensure a correct polarized mating (3.3 V or 5 V V(I/O) coding).

The CP3002 supports universal (3.3 V and 5 V) PCI V(I/O) signaling voltages with one common termination resistor configuration. Therefore, the CP3002 can be inserted in both, 3.3 V and 5 V CompactPCI systems and provides itself no guide lug.

Figure 2-5: CPCI Connectors J1/J2



2.11.10.2 CompactPCI Connectors J1 and J2 Pinouts

The CP3002 is provided with two 2 mm x 2 mm pitch female CompactPCI connectors, J1 and J2.

Table 2-12: CompactPCI Connector J1 System Controller Slot Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
25	NC	5V	REQ64#	ENUM#	3.3V	5V	GND
24	NC	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	NC	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	NC	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	NC	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	NC	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	NC	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	NC	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	NC	3.3V	RSV	RSV	GND	PERR#	GND
16	NC	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	NC	3.3V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
12-14	Key Area						
11	NC	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	NC	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	NC	C/BE[3]#	NC	AD[23]	GND	AD[22]	GND
8	NC	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	NC	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	NC	REQ0#	CPCI_PRESENT#	3.3V	CLK0	AD[31]	GND
5	NC	NC	NC	RST#	GND	GNT0#	GND
4	NC	NC	HEALTHY#	V(I/O)	RSV	RSV	GND
3	NC	INTA#	INTB#	INTC#	5V	INTD#	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	NC	TRST#	NC	5V	GND

The legacy IDE interrupts INTP (CompactPCI specification pin D4) and INTS (CompactPCI specification pin E4) are not implemented on the CP3002. Therefore, pins D4 and E4 are reserved.

The IPMB system management bus (CompactPCI specification pins A4, B17, C17) is not implemented on the CP3002. Therefore, pin A4 is not connected and pins B17 and C17 are reserved.

For further information regarding the above-mentioned reserved pins, please contact Kontron.

Table 2-13: CompactPCI Connector J1 Peripheral Slot Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
25	NC	5V	*	*	3.3V	5V	GND
24	NC	*	5V	V(I/O)	*	*	GND
23	NC	3.3V	*	*	5V	*	GND
22	NC	*	GND	3.3V	*	*	GND
21	NC	3.3V	*	*	*	*	GND
20	NC	*	GND	V(I/O)	*	*	GND
19	NC	3.3V	*	*	GND	*	GND
18	NC	*	GND	3.3V	*	*	GND
17	NC	3.3V	RSV	RSV	GND	*	GND
16	NC	*	*	V(I/O)	*	*	GND
15	NC	3.3V	*	*	BDSEL#	*	GND
14-12	Key Area						
11	NC	*	*	*	GND	*	GND
10	NC	*	GND	3.3V	*	*	GND
9	NC	*	NC	*	GND	*	GND
8	NC	*	GND	V(I/O)	*	*	GND
7	NC	*	*	*	GND	*	GND
6	NC	*	CPCI_PRESENT#	3.3V	*	*	GND
5	NC	NC	NC	RST#**	GND	*	GND
4	NC	NC	HEALTHY#	V(I/O)	RSV	RSV	GND
3	NC	*	*	*	5V	*	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	NC	TRST#	NC	5V	GND

Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP3002 is inserted in a peripheral slot.

** When the CP3002 is inserted in a peripheral slot, the function of the RST# signal can be enabled or disabled.

Table 2-14: 64-bit CompactPCI Connector J2 Pinout (CP3002 Front I/O Vers.)

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	CLK6	GND	RSV	RSV	RSV	GND
20	NC	CLK5	GND	RSV	RSV	RSV	GND
19	NC	GND	GND	RSV	RSV	RSV	GND
18	NC	RSV	RSV	RSV	RSV	RSV	GND
17	NC	RSV	RSV	PRST#	REQ6#	GNT6#	GND
16	NC	RSV	RSV	DEG#	RSV	RSV	GND
15	NC	RSV	RSV	FAL#	REQ5#	GNT5#	GND
14	NC	RSV	RSV	RSV	RSV	RSV	GND
13	NC	RSV	RSV	RSV	RSV	RSV	GND
12	NC	RSV	RSV	RSV	RSV	RSV	GND
11	NC	RSV	RSV	RSV	RSV	RSV	GND
10	NC	RSV	RSV	RSV	RSV	RSV	GND
9	NC	RSV	GND	RSV	RSV	RSV	GND
8	NC	RSV	RSV	RSV	GND	RSV	GND
7	NC	RSV	RSV	RSV	RSV	RSV	GND
6	NC	RSV	RSV	RSV	GND	RSV	GND
5	NC	RSV	GND	RSV	RSV	RSV	GND
4	NC	V(I/O)	RSV	RSV	RSV	RSV	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note ...

The 64-bit CompactPCI signals are not used on the board and the 64-bit control and address signals are not terminated to V(I/O).

2.11.10.3 Optional Rear I/O Interface

The CP3002 board provides optional rear I/O connectivity for peripherals. When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the rear I/O module interface.

The CP3002 with rear I/O is compatible with all standard 3U CompactPCI passive backplanes with rear I/O support.

Warning!

To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. Do not plug a rear I/O configured board in a backplane without rear I/O support. Failure to comply with the above will result in damage to your board.

The CP3002 rear I/O provides the following interfaces (all signals are available on J2 only if the board is ordered with rear I/O functionality):

- Two USB 2.0 ports
- Two Gigabit Ethernet ports without LED signals
- Two SATA ports
- Two COM ports (3.3 V LVTTL level)
- VGA analog port
- Management and control signals
- Input for +5V standby power
- Geographic addressing (GA[4..0])

Note ...

The pinout of the rear I/O CompactPCI connector on the CP3002 is compatible with that of the CP305, CP307, and CP308. Thus, rear I/O modules designed for these boards can also be used with the CP3002.

Table 2-15: Rear I/O CompactPCI Connector J2 Pinout (CP3002 Rear I/O Vers.)

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	CLK6	GND	USBA+	USBB+	USBA_PWR_5V	GND
20	NC	CLK5	GND	USBA-	USBB-	USBB_PWR_5V	GND
19	NC	GND	GND	PWR_BTN#	PWR_SLPS3#	RIO_3.3V	GND
18	NC	COMA_RXD	COMA_DCD#	COMA_DTR#	GPI1/ COMB_CTS#	COMA_CTS#	GND
17	NC	COMA_TXD	GPI0/ COMB_RXD	PRST#	REQ6#	GNT6#	GND
16	NC	COMA_DSR#	COMA_RTS#	DEG#	GND	COMA_RI#	GND
15	NC	PWR_5VSTD BY	RSV	FAL#	REQ5#	GNT5#	GND
14	NC	IPA_DA+	IPA_DA-	GPO1/ COMB_RTS#	IPA_DC+	IPA_DC-	GND
13	NC	IPA_DB+	IPA_DB-	GPI4/COMB_RI#	IPA_DD+	IPA_DD-	GND
12	NC	IPB_DA+	IPB_DA-	RIO_1V9	IPB_DC+	IPB_DC-	GND
11	NC	IPB_DB+	IPB_DB-	GPI3/ COMB_DCD#	IPB_DD+	IPB_DD-	GND
10	NC	NC	GPO0/ COMB_TXD	VGA_RED	GPO2/ COMB_DTR#	NC	GND
9	NC	SATAATX+	GND	VGA_HSYNC	NC	SATABTX+	GND
8	NC	SATAATX-	NC	VGA_BLUE	GND	SATABTX-	GND
7	NC	NC	GPI2/ COMB_DSR#	VGA_DDC_DATA	RSV	NC	GND
6	NC	SATAARX+	NC	VGA_GREEN	GND	SATABRX+	GND
5	NC	SATAARX-	GND	VGA_VSYNC	NC	SATABRX-	GND
4	NC	VI/O	RIO_5V	VGA_DDC_CLK	GPIO_CFG0	NC	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Table 2-16: Rear I/O Signal Description

SIGNAL	DESCRIPTION
COMAx	COMA port LVTTL (3.3V)
COMBx	COMB port LVTTL (3.3V)
GPI/GPO	General purpose input / general purpose output signal
GPIO_CFG0	GPIO or COMB configuration
IPx	Gigabit Ethernet copper port
SATAx	Serial ATA port
USBx	USB interface and power
VGAx	VGA signal
RIOx/VI/O	Power supply signal
PWRx	Power management signal
RSV	Reserved
GND	Ground signal
NC	Not connected

With the GPIO_CFG0 signal on the rear I/O module an active COMB or GPIO interface can be selected.

Table 2-17: GPIO Signal Description

GPIO SIGNAL	DESCRIPTION
GPIO_CFG0	0 = GPIO 1 = COMB

Note ...

The default value is 1 if pin D4 is not connected (pull-up resistor to 3.3V on CP3002). If the pin is connected, the default value depends on the rear I/O module. If the pin is driven by the rear I/O module, it must be considered that the CP3002 tolerates only 3.3 V signaling on this input.

2.11.10.4 Rear I/O Pin Description

Serial Ports

The CP3002 provides two serial ports, COMA and COMB, both available on the rear I/O CompactPCI connector J2.

Table 2-18: COMA and COMB Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
A17	COMA_TXD	TXD serial port (COMA)	CP3002	LVTTL (3.3V)
A18	COMA_RXD	RXD serial port (COMA)	Rear I/O module	LVTTL (3.3V)
E18	COMA_CTS#	CTS signal serial port (COMA)	Rear I/O module	LVTTL (3.3V)
B16	COMA_RTS#	RTS signal serial port (COMA)	CP3002	LVTTL (3.3V)
A16	COMA_DSR#	DSR signal serial port (COMA)	Rear I/O module	LVTTL (3.3V)
B18	COMA_DCD#	DCD signal serial port (COMA)	Rear I/O module	LVTTL (3.3V)
C18	COMA_DTR#	DTR signal serial port (COMA)	CP3002	LVTTL (3.3V)
E16	COMA_RI#	RI signal serial port (COMA)	Rear I/O module	LVTTL (3.3V)
B10	COMB_TXD	TXD serial port (COMB)	CP3002	LVTTL (3.3V)
B17	COMB_RXD	RXD serial port (COMB)	Rear I/O module	LVTTL (3.3V)
D18	COMB_CTS#	CTS signal serial port (COMB)	Rear I/O module	LVTTL (3.3V)
C14	COMB_RTS#	RTS signal serial port (COMB)	CP3002	LVTTL (3.3V)
B7	COMB_DSR#	DSR signal serial port (COMB)	Rear I/O module	LVTTL (3.3V)
C11	COMB_DCD#	DCD signal serial port (COMB)	Rear I/O module	LVTTL (3.3V)
D10	COMB_DTR#	DTR signal serial port (COMB)	CP3002	LVTTL (3.3V)
C13	COMB_RI#	RI signal serial port (COMB)	Rear I/O module	LVTTL (3.3V)

Note ...

The pins for the interfaces COMA and COMB (pins A18, A17, A16, B18, B17, B16, B10, B7, C18, C14, C13, C11, D18, D10, E18, and E16) tolerate only 3.3V signaling and their inputs (driven by the rear I/O module) have internal pull-up resistors.

General Purpose Inputs/Outputs

Alternatively, the following GPIO signals are available instead of the COMB signals if pin D4 on the rear I/O connector J2 (GPIO_CFG0) is set to 0.

Table 2-19: GPIO Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
B10	GPO0	General purpose output 0	CP3002	LVTTL (3.3V)
B17	GPI0	General purpose input 0	Rear I/O module	LVTTL (3.3V)
D18	GPI1	General purpose input 1	Rear I/O module	LVTTL (3.3V)
C14	GPO1	General purpose output 1	CP3002	LVTTL (3.3V)
B7	GPI2	General purpose input 2	Rear I/O module	LVTTL (3.3V)
C11	GPI3	General purpose input 3	Rear I/O module	LVTTL (3.3V)
D10	GPO2	General purpose output 2	CP3002	LVTTL (3.3V)
C13	GPI4	General purpose input 4	Rear I/O module	LVTTL (3.3V)

Note ...

The pins for the GPIO interface (pins B17, B10, B7, C14, C13, C11, D18, and D10) tolerate only 3.3 V signaling and their inputs (driven by the rear I/O module) have internal pull-up resistors.

VGA Interface

VGA signals are available either on the front VGA connector, J6, or on the rear I/O interface due to the implemented switch on the CP3002. Switching over from front to rear I/O or vice versa is effected using the uEFI BIOS or the board-specific Control Register 0 (0x282), bit 7-6 (default: front I/O).

Table 2-20: VGA Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
C10	VGA_RED	VGA analog red signal	CP3002	Analog
C6	VGA_GREEN	VGA analog green signal	CP3002	Analog
C8	VGA_BLUE	VGA analog blue signal	CP3002	Analog
C9	VGA_HSYNC	VGA horizontal synchronization signal	CP3002	LVTTL (3.3 V)
C5	VGA_VSYNC	VGA vertical synchronization signal	CP3002	LVTTL (3.3 V)
C4	VGA_DDC_CLK	Monitor control clock signal	CP3002	TTL (5 V)
C7	VGA_DDC_DATA	Monitor control data signal	Bidirectional	TTL (5 V)

Note ...

On the rear I/O, the CP3002 provides 150 Ω termination resistors for the red, green and blue VGA signals. Thus, further 150 Ω termination resistors are necessary on the rear I/O module to reach the required 75 Ω termination for the VGA connection.

Ethernet Interfaces

Gigabit Ethernet signals are available either on the front RJ-45 connector or on the rear I/O interface due to the implemented switches on the CP3002. Both Gigabit Ethernet channels are individually switchable to front or rear I/O. Switching over from front to rear I/O or vice versa is effected using the uEFI BIOS settings (default: front I/O).

Table 2-21: Gigabit Ethernet Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
A14	IPA_DA+	Media-dependent interface port A	Bidirectional	Analog
B14	IPA_DA-	Media-dependent interface port A	Bidirectional	Analog
A13	IPA_DB+	Media-dependent interface port A	Bidirectional	Analog
B13	IPA_DB-	Media-dependent interface port A	Bidirectional	Analog
D14	IPA_DC+	Media-dependent interface port A	Bidirectional	Analog
E14	IPA_DC-	Media-dependent interface port A	Bidirectional	Analog
D13	IPA_DD+	Media-dependent interface port A	Bidirectional	Analog
E13	IPA_DD-	Media-dependent interface port A	Bidirectional	Analog
A12	IPB_DA+	Media-dependent interface port B	Bidirectional	Analog
B12	IPB_DA-	Media-dependent interface port B	Bidirectional	Analog
A11	IPB_DB+	Media-dependent interface port B	Bidirectional	Analog
B11	IPB_DB-	Media-dependent interface port B	Bidirectional	Analog
D12	IPB_DC+	Media-dependent interface port B	Bidirectional	Analog
E12	IPB_DC-	Media-dependent interface port B	Bidirectional	Analog
D11	IPB_DD+	Media-dependent interface port B	Bidirectional	Analog
E11	IPB_DD-	Media-dependent interface port B	Bidirectional	Analog
C12	RIO_1V9	Power supply for magnetics center tap	CP3002	1.9V

Note ...

The Ethernet magnetics must be placed on the rear I/O module. The Ethernet magnetics center tap must be connected to the dedicated 1.9 V power supply provided by the CP3002 (pin C12 on J2).

Warning!

Pin C12 is a power supply **OUTPUT**. This pin **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Serial ATA Interfaces

The CP3002 provides two Serial ATA interfaces on the rear I/O CompactPCI connector J2.

Table 2-22: Serial ATA Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
A6	SATAARX+	Positive input port A	Rear I/O module	Differential
A5	SATAARX-	Negative input port A	Rear I/O module	Differential
A9	SATAATX+	Positive output port A	CP3002	Differential
A8	SATAATX-	Negative output port A	CP3002	Differential
E6	SATABRX+	Positive input port B	Rear I/O module	Differential
E5	SATABRX-	Negative input port B	Rear I/O module	Differential
E9	SATABTX+	Positive output port B	CP3002	Differential
E8	SATABTX-	Negative output port B	CP3002	Differential

USB Interfaces

Two USB 2.0 ports are available on the rear I/O CompactPCI connector J2.

Table 2-23: USB Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
C21	USBA+	Positive USB port A	Bidirectional	Differential
C20	USBA-	Negative USB port A	Bidirectional	Differential
E21	USBA_PWR_5V	USB power supply 5 V port A	CP3002	5 V
D21	USBB+	Positive USB port B	Bidirectional	Differential
D20	USBB-	Negative USB port B	Bidirectional	Differential
E20	USBB_PWR_5V	USB power supply 5 V port B	CP3002	5 V

Power Supply and Power Management Signals

The CP3002 provides the following power supply and power management signals to the rear I/O module.

Table 2-24: Power Supply and Power Management Signal Description

PIN on J2	SIGNAL	FUNCTION	DRIVEN BY	SIGNALING VOLTAGE
B4	RIO_5V	Power supply 5 V	CP3002	5 V
E19	RIO_3.3V	Power supply 3.3 V	CP3002	3.3 V
A4	VI/O	Power supply VI/O	Backplane	5 V or 3.3 V
A15	PWR_5V_STDBY	Power supply 5 V standby	Rear I/O module	5 V
C19	PWR_BTN#	Power button signal	Rear I/O module	Open drain (pull-up resistor on the CP3002) or LVTTL (3.3 V)
D19	PWR_SLPS3#	Sleep S3 signal	CP3002	LVTTL (3.3 V)
B15, D7	RSV	Reserved	--	--

Warning!

Pins B15 and D7 **MUST NOT** be connected to any signal, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Warning!

Pins B4 and E19 are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

For further information regarding the rear I/O signals, please contact Kontron.

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Chapter 3

Installation

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3. Installation

The CP3002 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP3002. *Kontron* assumes no responsibility for any damage resulting from failure to comply with these requirements.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

Caution!

If your board type is not specifically qualified as being hot swap capable, switch off the CompactPCI system power before installing the board in a free CompactPCI slot. Failure to do so could endanger your life or health and may damage your board or system.

Note ...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

3.2 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP3002 in a system. Procedures for standard removal and insertion/removal under power are found in their respective chapters.

To perform an initial installation of the CP3002 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed.

Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP3002 refer to Chapter 4. For the installation of CP3002-specific peripheral devices and rear I/O devices refer to the appropriate sections in Chapter 3.

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP3002 nor other system boards are physically damaged by the application of these procedures.

3. To install the CP3002 perform the following:
   1. Ensure that no power is applied to the system before proceeding.

Warning!

Even though power may be removed from the system, the CP3002 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handle to seat the board into the backplane connectors.

   2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
4. Fasten the front panel retaining screws.
5. Connect all external interfacing cables to the board as required.
6. Ensure that the board and all required interfacing cables are properly secured.

The CP3002 is now ready for initial operation. Except for the uEFI BIOS, at this point there is no other software installed. For software installation and further operation of the CP3002, refer to appropriate CP3002 software (uEFI BIOS, BSP, OS), application, and system documentation.

3.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP3002 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.

Warning!

Even though power may be removed from the system, the CP3002 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handle and then by pressing the handle as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

3.4 Insertion/Removal under Power

The CP3002 is designed for use either as a CompactPCI system controller or as an autonomous CPU board in a CompactPCI peripheral slot.

When installed in the system controller slot, the CP3002 provides all required functions for supporting the hot swapping of peripheral boards which are capable of being hot swapped. In this configuration the CP3002 itself is not hot-swappable.

When installed in a CompactPCI peripheral slot, the CP3002 operates autonomously, meaning that it only draws power from the CompactPCI backplane. There is no interfacing with the CompactPCI bus, clocks or other control signals. In this configuration, the CP3002 supports hot plugging. This simply means that the board can be installed or removed from the system while under power.

Warning!

Always ensure that all functions in progress are properly terminated or put into a safe state prior to hot plugging the CP3002.

Failure to comply with the above may result in improper operation or damage to other system components, e.g. operating system failure, data loss, uncontrolled processing, etc.

Note ...

In order to use the hot plug function of the CP3002, a hot swap-capable backplane is required.

3.4.1 Replacement under Power in Peripheral Slot

This procedure assumes that the system supports hot plugging, and that the replacement for the board to be hot plugged is configured hardware- and software-wise for operation in the application.

To replace the CP3002 proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP3002 nor other system boards are physically damaged by the application of these procedures.

2. Ensure that the board may be removed from the system.

Note ...

The performance of this step is a function of the application. Consult the application description/procedure for determining when the CP3002 board may be removed from the system.

3. Disconnect any interfacing cables that may be connected to the board.

Warning!

The CP3002 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

4. Unscrew the front panel retaining screws.
5. Unlock the ejector handle.
6. Using the ejector handle, disengage the board from the backplane and carefully remove it from the system.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the “old” board as required observing the safety requirements indicated in Chapter 3.1.
8. Obtain the replacement CP3002 board.

Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handle to seat the board into the backplane connectors.

9. Carefully insert the “new” board into the “old” board slot until it makes contact with the backplane connectors.
10. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
11. Fasten the front panel retaining screws.

12. Connect all required interfacing cables to the board.

Warning!

The CP3002 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

Replacement of the CP3002 under power is now complete.

3.5 Installation of CP3002 Peripheral Devices

The CP3002 is designed to accommodate various peripheral devices, such as USB devices, Serial ATA devices, a CFast card, etc. The following figures show the placement of modules and peripheral devices on the CP3002.

Figure 3-1: Connecting a Peripheral Device to the 4HP CP3002

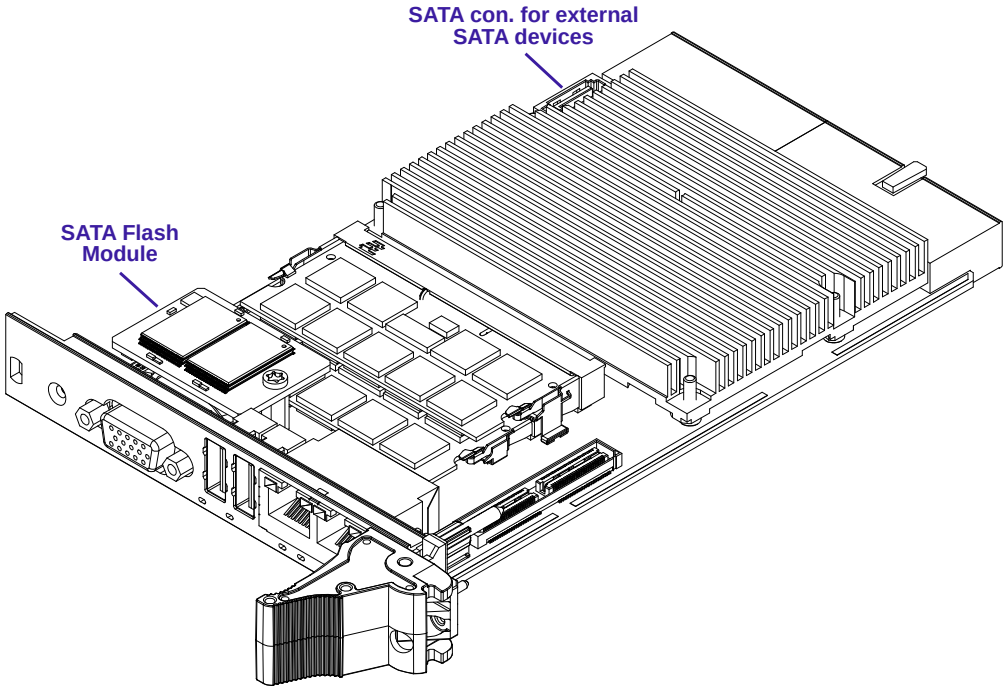
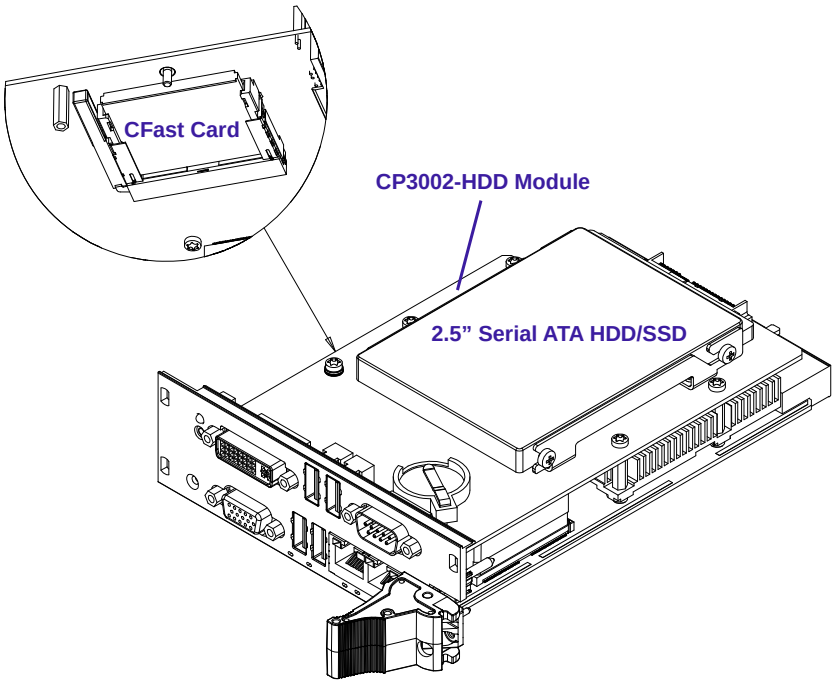


Figure 3-2: Connecting a Peripheral Device to the 8HP CP3002 with CP3002-HDD



The following chapters provide information regarding installation aspects of peripheral devices.

3.5.1 USB Device Installation

The CP3002 supports all USB Plug and Play computer peripherals (e.g. keyboard, mouse, printer, etc.).

Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.

3.5.2 Installation of External Serial ATA Devices

The following information pertains to external SATA devices which may be connected to the CP3002 via normal cabling.

Some symptoms of incorrectly installed SATA devices are:

- Device on a SATA channel does not spin up: check power cables and cabling. May also result from a bad power supply or SATA device.
  The SATA connector on the CP3002 provides only a data connection. The power for this device must be supplied by a separate connector. For further information, refer to the respective documentation of the device.
- SATA device fail message at boot-up: may be a bad cable or lack of power going to the drive.

3.5.3 SATA Flash Module Installation

A SATA Flash module may be connected to the 4HP CP3002 via the onboard connector J5.

This optionally available module must be physically installed on the CP3002 prior to installation of the CP3002 in a system.

During installation it is necessary to ensure that the SATA Flash module is properly seated in the onboard connector J5, i.e. the pins are aligned correctly and not bent, prior to fixing the SATA Flash module with the respective screw

Note ...

Only qualified SATA Flash modules from Kontron are authorized for use with the CP3002. Failure to comply with the above will void the warranty and may result in damage to the board or the system.

The SATA Flash module cannot be used in conjunction with the CP3002-HDD module.

3.5.4 2.5” HDD/SSD Installation

One 2.5” SATA HDD/SSD may be connected to the 8HP CP3002 via the CP3002-HDD and the respective SATA connector. For further information regarding the CP3002-HDD module, refer to Appendix A in this manual.

3.5.5 CFast Card Installation

The 8HP CP3002 equipped with the CP3002-HDD module provides a CFast card socket with ejector. For further information regarding the CP3002-HDD module, refer to Appendix A in this manual.

Note ...

The CP3002-HDD does not support removal and reinsertion of the CFast storage card while the board is in a powered-up state. Connecting the CFast card while the power is on, which is known as "hot plugging", may damage your system.

3.5.6 Rear I/O Device Installation

For physical installation of rear I/O devices, refer to the documentation provided with the device itself.

Note ...

VGA and Ethernet can be used either on the front panel or on the rear I/O. COMA can be used either on the 8HP expansion module or on the rear I/O. It is not possible to use any of the above-mentioned interfaces on the front or the 8HP expansion and on the rear I/O simultaneously.

3.5.7 Battery Replacement

The CP3002 is provided with a 3.0 V “coin cell” lithium battery for the RTC. The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery type is CR2025.

To replace the battery, proceed as follows:

- Turn off power.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

Note ...

The user must be aware that the battery’s operational temperature range is less than the CP3002’s storage temperature range.

For exact range information, refer to the battery manufacturer’s specifications.

Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer’s instructions.

The typical life expectancy of a 170 mAh battery (CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 4 - 5 years.

3.6 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

Note ...

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems, for example Windows® XP, Windows® XP Embedded, must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.

Chapter 4

Configuration

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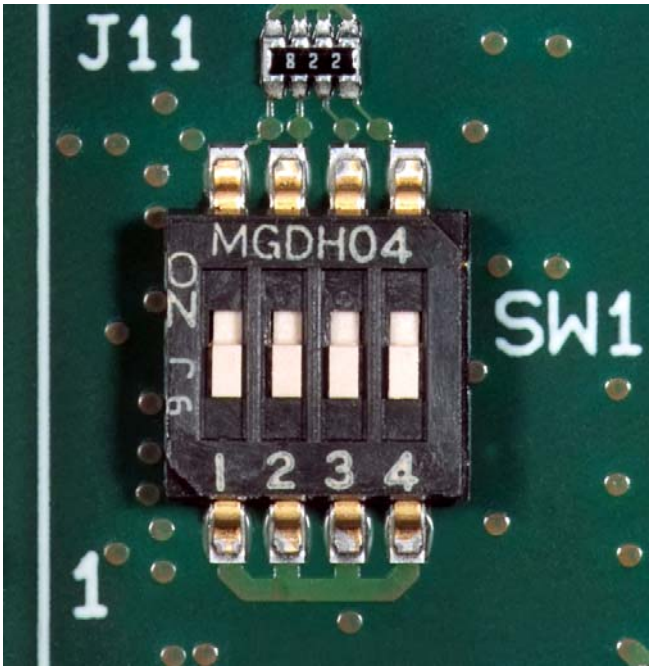
4. Configuration

4.1 DIP Switch Configuration

The DIP switch consists of four switches for board configuration: switch 1 for POST code indication on LED0..3, switch 2 for the SPI boot flash configuration, switch 3 for reset configuration, and switch 4 for the uEFI BIOS configuration.

Figure 4-1: DIP Switch SW1



The following table indicates the functionality of the four switches integrated in the DIP switch.

Table 4-1: DIP Switch SW1 Functionality

SWITCH	SETTING	FUNCTIONALITY
1	*OFF*	*Boot-up with POST code indication on LED0..3*
	ON	Boot-up with no POST code indication on LED0..3
2	*OFF*	*Boot from the default SPI boot flash*
	ON	Boot from the alternative SPI boot flash
3	*OFF*	*Edge-sensitive reset configuration (QM57 reset implementation)*
	ON	Level-sensitive reset configuration (FPGA PGOOD logic to QM57)
4	*OFF*	*Boot using the currently saved uEFI BIOS settings*
	ON	Clear the uEFI BIOS settings and use the default values

The default setting is indicated by using italic bold.

To clear the uEFI BIOS settings and the passwords, proceed as follows:

1. Set DIP switch SW1, switch 4, to the ON position.
2. Apply power to the system.
3. Wait 30 seconds and then remove power from the system. During this time period no messages are displayed.
4. Set DIP switch SW1, switch 4, to the OFF position.

4.2 Jumper Description

The CP3002 has two solder jumpers, one reserved for factory use (JP1) and one reserved for future use (JP2).

4.2.1 I/O Address Map

The following table indicates the CP3002-specific registers.

Table 4-2: I/O Address Map

ADDRESS	DEVICE
0x080	uEFI BIOS POST Code Low Byte Register (POSTL)
0x081	uEFI BIOS POST Code High Byte Register (POSTH)
0x082 - 0x083	Reserved
0x084	Debug Low Byte Register (DBGL)
0x085	Debug High Byte Register (DBGH)
0x280	Status Register 0 (STAT0)
0x281	Status Register 1 (STAT1)
0x282	Control Register 0 (CTRL0)
0x283	Control Register 1 (CTRL1)
0x284	Device Protection Register (DPROT)
0x285	Reset Status Register (RSTAT)
0x286	Board Interrupt Configuration Register (BICFG)
0x287	Status Register 2 (STAT2)
0x288	Board ID High Byte Register (BIDH)
0x289	Board and PLD Revision Register (BREV)
0x28A	Geographic Addressing Register (GEOAD)
0x28B	Reserved
0x28C	Watchdog Timer Control Register (WTIM)
0x28D	Board ID Low Byte Register (BIDL)
0x28E - 0x28F	Reserved
0x290	LED Configuration Register (LCFG)
0x291	LED Control Register (LCTRL)
0x292	General Purpose Output Register (GPOUT)
0x293	General Purpose Input Register (GPIN)
0x294 - 0x29F	Reserved

4.3 CP3002-Specific Registers

The following registers are special registers which the CP3002 uses to watch the onboard hardware special features and a number of CompactPCI control signals.

Normally, only the system uEFI BIOS uses these registers, but they are documented here for application use as required.

Note ...

Take care when modifying the contents of these registers as the system uEFI BIOS may be relying on the state of the bits under its control.

4.3.1 Status Register 0 (STAT0)

The Status Register 0 holds general/common status information.

Table 4-3: Status Register 0 (STAT0)

REGISTER NAME		STATUS REGISTER 0 (STAT0)		
ADDRESS		0x280		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	Res.	Reserved	0	R
6	BBEI	uEFI BIOS boot end indication: 0 = uEFI BIOS is booting 1 = uEFI BIOS boot is finished	0	R
5 - 4	BFSS	Boot flash selection status: 00 = Standard boot flash active 01 = Recovery boot flash active 10 = External boot flash active 11 = Reserved	N/A	R
3	DIP4	DIP switch SW1, switch 4 (clear the uEFI BIOS settings): 0 = Switch on 1 = Switch off	N/A	R
2	DIP3	DIP switch SW1, switch 3 (reset configuration): 0 = Switch on 1 = Switch off	N/A	R
1	DIP1	DIP switch SW1, switch 2 (select SPI boot flash): 0 = Switch on 1 = Switch off	N/A	R
0	DIP0	DIP switch SW1, switch 1 (POST code indication on LED0..3): 0 = Switch on 1 = Switch off	N/A	R

4.3.2 Status Register 1 (STAT1)

The Status Register 1 holds board-specific status information.

Table 4-4: Status Register 1 (STAT1)

REGISTER NAME		STATUS REGISTER 1 (STAT1)		
ADDRESS		0x281		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	Res.	Reserved	0000	R
3	CSYS	CPCI system slot identification (SYSEN signal): 0 = Installed in a system slot 1 = Installed in a peripheral slot	N/A	R
2	CENUM	CPCI system enumeration (ENUM signal): 0 = Indicates the insertion or removal of a hot swap peripheral board when the CP3002 operates as the system controller board 1 = No hot swap event	N/A	R
1	CFAL	CPCI power supply status (FAL signal): 0 = Power supply failure 1 = Power in normal state	N/A	R
0	CDEG	CPCI power supply status (DEG signal): 0 = Power derating 1 = Power in normal state	N/A	R

4.3.3 Control Register 0 (CTRL0)

The Control Register 0 holds a series of bits defining general/common configuration functions.

Table 4-5: Control Register 0 (CTRL0)

REGISTER NAME		CONTROL REGISTER 0 (CTRL0)		
ADDRESS		0x282		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 6	VGAM	VGA mode configuration: 00 = Automatic VGA front detection 01 = Front VGA (uEFI BIOS default) 10 = Rear VGA 11 = VGA disabled	01	R/W
5	BFUS	Boot flash update selection: 0 = Select default boot flash for update 1 = Select alternative boot flash for update	0	R/W
4 - 0	Res.	Reserved	00000	R

4.3.4 Control Register 1 (CTRL1)

The Control Register 1 holds board-specific control information.

Table 4-6: Control Register 1 (CTRL1)

REGISTER NAME		CONTROL REGISTER 1 (CTRL1)		
ADDRESS		0x283		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	SRST	SATA Flash module configuration: 0 = Reset of SATA Flash module 1 = SATA Flash module running	1	R/W
6	VRST	Integrated graphics controller configuration: 0 = Graphics controller disabled 1 = Graphics controller enabled	1	R
5	TRST	Trusted Platform Module (TPM) configuration: 0 = TPM disabled 1 = TPM enabled	1	R/W
4	CRST	CPCI reset in peripheral slot: 0 = Disable CPCI reset to board 1 = Enable CPCI reset to board	0	R/W
3	Res.	Reserved	0	R
2	SCOMA	COMA routing selection: 0 = Rear I/O 1 = 8HP expansion module	N/A (see note below)	R/W
1 - 0	Res.	Reserved	00	R

Note ...

The reset value of the SCOMA bit depends on the board version ordered. If the CP3002 is ordered as a rear I/O version, the reset value is 0. If the CP3002 is ordered as a front I/O version, an automatic switch over to the 8HP expansion module is processed per default.

4.3.5 Device Protection Register (DPROT)

The Device Protection Register holds the write protect signals for flash devices.

Table 4-7: Device Protection Register (DPROT)

REGISTER NAME		DEVICE PROTECTION REGISTER (DPROT)		
ADDRESS		0x284		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 3	Res.	Reserved	00000	R
2	SFWP	SATA Flash module write protection: 0 = SATA Flash module not write protected 1 = SATA Flash module write protected Writing a '1' to this bit sets the bit. If this bit is set, it cannot be cleared.	0	R/W
1	EEWP	EEPROM write protection: 0 = EEPROM not write protected 1 = EEPROM write protected Writing a '1' to this bit sets the bit. If this bit is set, it cannot be cleared.	0	R/W
0	BFWP	SPI boot flash write protection: 0 = SPI boot flash not write protected 1 = SPI boot flash write protected Writing a '1' to this bit sets the bit. If this bit is set, it cannot be cleared.	0	R/W

4.3.6 Reset Status Register (RSTAT)

The Reset Status Register is used to determine the host's reset source.

Table 4-8: Reset Status Register (RSTAT)

REGISTER NAME		RESET STATUS REGISTER (RSTAT)		
ADDRESS		0x285		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	PORS	Power-on reset status: 0 = System reset generated by software (warm reset) 1 = System reset generated by power-on (cold reset) Writing a '1' to this bit clears the bit.	N/A	R/W
6 - 3	Res.	Reserved	0000	R
2	FPRS	Front panel push button reset status (CP3002-HDD): 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' to this bit clears the bit.	0	R/W
1	CPRS	CompactPCI reset status (PRST signal): 0 = System reset not generated by CPCI reset input 1 = System reset generated by CPCI reset input Writing a '1' to this bit clears the bit.	0	R/W
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.	0	R/W

Note ...

The Reset Status Register is set to the default values by power-on reset, not by a warm reset.

4.3.7 Board Interrupt Configuration Register (BICFG)

The Board Interrupt Configuration Register holds a series of bits defining the interrupt routing.

Table 4-9: Board Interrupt Configuration Register (BICFG)

REGISTER NAME		BOARD INTERRUPT CONFIGURATION REGISTER (BICFG)		
ADDRESS		0x286		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	UICF	UART IRQ3 and IRQ4 interrupt configuration: 0 = Disabled 1 = Enabled	1	R/W
6	CFICF	CPCI fail signal interrupt configuration (FAL signal): 0 = IRQ5 disabled 1 = IRQ5 enabled	0	R/W
5	CEICF	CPCI enumeration signal interrupt configuration (ENUM signal): 0 = IRQ5 disabled 1 = IRQ5 enabled	0	R/W
4	CDICF	CPCI derate signal interrupt configuration (DEG signal): 0 = IRQ5 disabled 1 = IRQ5 enabled	0	R/W
3 - 2	Res.	Reserved	00	R
1 - 0	WICF	Watchdog interrupt configuration: 00 = Disabled 01 = IRQ5 10 = Reserved 11 = Reserved	00	R/W

4.3.8 Status Register 2 (STAT2)

The Status Register 2 holds status information related to the rear I/O configuration.

Table 4-10: Status Register 2 (STAT2)

REGISTER NAME		STATUS REGISTER 2 (STAT2)		
ADDRESS		0x287		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 6	Res.	Reserved	00	R
5 - 4	RCFG	Rear I/O configuration: 00 = Rear I/O disabled (CP3002 front I/O version) 01 = COMA, GPIO 10 = Reserved 11 = COMA, COMB The default value depends on the CP3002 version ordered (front I/O or rear I/O) and the rear I/O module used.	N/A	R
3 - 0	Res.	Reserved	0000	R

4.3.9 Board ID High Byte Register (BIDH)

Each Kontron board is provided with a unique 16-bit board-type identifier in the form of a hexadecimal number.

Table 4-11: Board ID High Byte Register (BIDH)

REGISTER NAME		BOARD ID HIGH BYTE REGISTER (BIDH)		
ADDRESS		0x288		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BIDH	Board identification: CP3002: 0xB320	0xB3	R

Note ...

The Board ID Low Byte Register is located in the address 0x28D.

4.3.10 Board and PLD Revision Register (BREV)

The Board and PLD Revision Register signals to the software when differences in the board and the Programmable Logic Device (PLD) require different handling by the software. It starts with the value 0x00 and will be incremented with each change in hardware as development continues.

Table 4-12: Board and PLD Revision Register (BREV)

REGISTER NAME		BOARD AND PLD REVISION REGISTER (BREV)		
ADDRESS		0x289		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	BREV	Board revision	N/A	R
3 - 0	PREV	PLD revision	N/A	R

4.3.11 Geographic Addressing Register (GEOAD)

This register holds the CompactPCI geographic address.

Table 4-13: Geographic Addressing Register (GEOAD)

REGISTER NAME		GEOGRAPHIC ADDRESSING REGISTER (GEOAD)		
ADDRESS		0x28A		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 5	Res.	Reserved	000	R
4 - 0	GA	Geographic address	N/A	R

4.3.12 Watchdog Timer Control Register (WTIM)

The CP3002 has one Watchdog timer provided with a programmable timeout ranging from 125 msec to 4096 sec. Failure to strobe the Watchdog timer within a set time period results in a system reset or an interrupt. The interrupt mode can be configured via the Board Interrupt Configuration Register (0x286).

There are four possible modes of operation involving the Watchdog timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Timer Control Register must be set according to the application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode changed by powering down and then up again. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a ’1’ to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to ’1’. What transpires after this depends on the mode selected.

The four operational Watchdog timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a ’1’ to the WTR bit. In the event a timeout occurs, the WTE bit is set to ’1’. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a ’1’ to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. If the Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.

Table 4-14: Watchdog Timer Control Register (WTIM)

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER (WTIM)		
ADDRESS		0x28C		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	WTE	Watchdog timer expired status bit 0 = Watchdog timer has not expired 1 = Watchdog timer has expired. Writing a '1' to this bit resets it to 0.	0	R/W
6 - 5	WMD	Watchdog mode 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)	00	R/W
4	WEN/WTR	Watchdog enable / Watchdog trigger control bit: 0 = Watchdog timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog timer is enabled, it will indicate a '1'. 1 = Watchdog timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].	0	R/W
3 - 0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = 512 s 1101 = 1024 s 1110 = 2048 s 1111 = 4096 s	0000	R/W

4.3.13 Board ID Low Byte Register (BIDL)

Each Kontron board is provided with a unique 16-bit board-type identifier in the form of a hexadecimal number. The following register indicates the low byte value of the board ID.

Table 4-15: Board ID Low Byte Register (BIDL)

REGISTER NAME		BOARD ID LOW BYTE REGISTER (BIDL)		
ADDRESS		0x28D		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BIDL	Board identification: CP3002: 0xB320	0x20	R

Note ...

The Board ID High Byte Register is located in the address 0x288.

4.3.14 LED Configuration Register (LCFG)

The LED Configuration Register holds a series of bits defining the onboard configuration for the front panel General Purpose LEDs.

Table 4-16: LED Configuration Register (LCFG)

REGISTER NAME		LED CONFIGURATION REGISTER (LCFG)		
ADDRESS		0x290		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	Res.	Reserved	0000	R
3 - 0	LCON	LED0..3 configuration: 0000 = POST [1)] 0001 = General Purpose Mode[2)] 0010 - 1111 = Reserved	0000	R/W

[1)] In uEFI BIOS POST mode, the LED0..3 build a binary vector to display uEFI BIOS POST code during the pre-boot phase. In doing so, the higher 4-bit nibble of the 8-bit uEFI BIOS POST code is displayed followed by the lower nibble followed by a pause. uEFI BIOS POST code is displayed in general in green color.

LED3: POST bit 3 and bit 7 (green)
LED2: POST bit 2 and bit 6 (green)
LED1: POST bit 1 and bit 5 (green)
LED0: POST bit 0 and bit 4 (green)

For further information reading the 8-bit uEFI BIOS POST Code, refer to Chapter 2.11.1.2, “General Purpose LEDs”.

[2)] Configured for General Purpose Mode, the LEDs are dedicated to functions as follows:

LED3: LED3 controlled by HOST (red/green/red+green)
LED2: LED2 controlled by HOST (red/green/red+green)
LED1: LED1 controlled by HOST (red/green/red+green)
LED0: LED0 controlled by HOST (red/green/red+green)

Beside the configurable functions described above, the LED0..3 fulfill also a basic debug function during the power-up phase as long as the first access to Port 80 is processed. If an LED lights red and stays red, than a basic error is present on the board. The following debug functions are defined and displayed during this initialization phase.

LED3: Power good status not reached (red)
LED2: Processor catastrophic error (red)
LED1: Hardware reset active/not deactivated (red)
LED0: uEFI BIOS boot failure (red)

4.3.15 LED Control Register (LCTRL)

The LED Control Register enables the user to switch on and off the front panel General Purpose LEDs.

Table 4-17: LED Control Register (LCTRL)

REGISTER NAME		LED CONTROL REGISTER (LCTRL)		
ADDRESS		0x291		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	LCMD	LED command: 0000 = Get LED0 0001 = Get LED1 0010 = Get LED2 0011 = Get LED3 0100 - 0111 = Reserved 1000 = Set LED0 1001 = Set LED1 1010 = Set LED2 1011 = Set LED3 1100 - 1111 = Reserved	0000	R/W
3 - 0	LCOL	LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Red+Green 0100 - 1111 = Reserved	0000	R/W

Note ...

This register can only be used if the General Purpose LEDs indicated in the “LED Configuration Register” (Table 4-16) are configured in General Purpose Mode.

4.3.16 General Purpose Output Register (GPOUT)

The General Purpose Output Register holds the general purpose output signals of the rear I/O CompactPCI connector J2. This register can be used only if the CP3002 is ordered as a rear I/O version and the rear I/O GPIO operation is configured through the dedicated rear I/O module configuration signal on the CompactPCI J2 connector.

Table 4-18: General Purpose Output Register (GPOUT)

REGISTER NAME		GENERAL PURPOSE OUTPUT REGISTER (GPOUT)		
ADDRESS		0x292		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 3	Res.	Reserved	00000	R
2	GPO2	General purpose output 2 signal (3.3V LVTTL): 0 = Output low 1 = Output high	0	R/W
1	GPO1	General purpose output 1 signal (3.3V LVTTL): 0 = Output low 1 = Output high	0	R/W
0	GPO0	General purpose output 0 signal (3.3V LVTTL): 0 = Output low 1 = Output high	0	R/W

4.3.17 General Purpose Input Register (GPIN)

The General Purpose Input Register holds the general purpose input signals of the rear I/O CompactPCI connector J2. This register can be used only if the CP3002 is ordered as a rear I/O version and the rear I/O GPIO operation is configured through the dedicated rear I/O module configuration signal on the CompactPCI J2 connector.

Table 4-19: General Purpose Input Register (GPIN)

REGISTER NAME		GENERAL PURPOSE INPUT REGISTER (GPIN)		
ADDRESS		0x293		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 5	Res.	Reserved	000	R
4	GPI4	General purpose input 4 signal (3.3V LVTTL): 0 = Input low 1 = Input high	1	R
3	GPI3	General purpose input 3 signal (3.3V LVTTL): 0 = Input low 1 = Input high	1	R
2	GPI2	General purpose input 2 signal (3.3V LVTTL): 0 = Input low 1 = Input high	1	R
1	GPI1	General purpose input 1 signal (3.3V LVTTL): 0 = Input low 1 = Input high	1	R
0	GPI0	General purpose input 0 signal (3.3V LVTTL): 0 = Input low 1 = Input high	1	R

Note ...

The CP3002 provides pull-up resistors on the rear I/O signal pins GPI[4:0], which leads to the default setting “input high” if the inputs are not connected.

The general purpose inputs support 3.3 V LVTTL signaling only (not 5V friendly).

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Chapter 5

Power Considerations

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5. Power Considerations

5.1 System Power

The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the CP3002 system environment.

5.1.1 CP3002 Baseboard

The CP3002 baseboard itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP3002 should be carefully tested to ensure compliance with these ratings.

Table 5-1: Maximum Input Power Voltage Limits

SUPPLY VOLTAGE	MAXIMUM PERMITTED VOLTAGE
+3.3 V	+3.6 V
+5 V	+5.5 V
+5 V STDBY (optional)	+5.5 V

Warning!

The maximum permitted voltages indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP3002 is not guaranteed to function if the board is operated beyond the prescribed limits.

Table 5-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.
+5 V STDBY (optional)	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.

5.1.2 Backplane

Backplanes to be used with the CP3002 must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V and +5 V power inputs.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

5.1.3 Power Supply Units

Power supplies for the CP3002 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the CP3002 has been optimized for minimal power consumption, the power supply unit must be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for backplane input line resistance variations due to temperature changes, etc.

Note ...

Non-industrial ATX PSUs may require a greater minimum load than a single CP3002 is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP3002 may hang up. The solution is to use an industrial PSU or to add more load to the system.

5.1.3.1 Start-Up Requirement

Power supplies must comply with the following guidelines, in order to be used with the CP3002.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

5.1.3.2 Power-Up Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

Both voltages must reach their minimum in-regulation level not later than 20 ms after the output power ramp start.

5.1.3.3 Tolerance

The tolerance of the voltage lines is described in the CPCI specification (PICMG 2.0 R3.0).The recommended measurement point for the voltage is the CPCI connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

Table 5-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)	REMARKS
+5 V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
+3.3 V	+3.3 VDC	+5%/-3%	50 mV	Main voltage
+12 V	+12 VDC	+5%/-5%	240 mV	Not required
-12 V	-12 VDC	+5%/-5%	240 mV	Not required
V I/O (PCI) signalling voltage	+3.3 VDC or +5 VDC	+5%/-3%	50 mV	--
+5 V STDBY	+5.0 VDC	+5%/-3%	50 mV	Optional voltage over J2 con.
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

5.1.3.4 Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Warning!

All of the input voltages must be functionally coupled to each other so that if one input voltage fails, all other input voltages must be regulated proportionately to the failed voltage. For example, if the +5V begins to decrease, all other input voltages must decrease accordingly. This is required in order to preclude cross currents within the CP3002.

Failure to comply with above may result in damage to the board or improper system operation.

Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until the capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP3002 baseboard and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and the power specifications for the CP3002 board and its accessories. The values were measured using an 8-slot passive CompactPCI backplane with two power supplies, one for the CPU, and the other for the hard disk and the CompactPCI system fans.

The operating systems used were uEFI shell and Windows® XP, 32-bit. The Core™ i7 processors had Intel® Turbo Boost Technology and Intel® Intelligent Power Sharing enabled. All measurements were conducted at a temperature of 25°C. The measured values varied, because the power consumption was dependent on the processor activity.

Note ...

The power consumption values indicated in the tables below can vary depending on the ambient temperature or the system performance. This can result in deviations of the power consumption values of up to 10%.

The power consumption was measured using the following processors:

- Intel® Core™ i7-660UE (ULV), 1.33 GHz, 4 MB L3 cache
- Intel® Core™ i7-620LE (LV), 2.0 GHz, 4 MB L3 cache
- Intel® Core™ i7-610E (SV), 2.53 GHz, 4 MB L3 cache
- Intel® Celeron® U3405 (ULV), 1.07 GHz, 2 MB L3 cache

with the following firmware and under the following testing conditions:

- CP3002 in EFI shell
  For this measurement the processor cores were active (no power management enabled) and the graphics controller was in idle state (no application running).
- CP3002 with Windows® XP, 32-bit, processor and graphics controller in idle state
  For this measurement all processor cores and the graphics controller were in idle state (power management enabled and no application running).
- CP3002 with Windows® XP, 32-bit, maximum processor workload with graphics controller in idle state
  For this measurement all processor cores were operating at maximum workload and the graphics controller was in idle state (e.g. dual screen output configuration with no video application running). These values represent the power dissipation reached under realistic, OS-controlled applications with the processor operating at maximum performance.
- CP3002 with Win.® XP, 32-bit, maximum processor and graphics controller workload
  These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor and graphics controller. These values are unlikely to be reached in real applications.

The following tables indicate the power consumption of the CP3002 with 4 GB DDR3 SDRAM memory with ECC (one 2 GB SODIMM module with ECC in each DDR3 SODIMM socket). The measurements were made with the CP3002 in EFI Shell mode as well as with the Windows® XP operating system, 32-bit.

Table 5-4: CP3002 in EFI Shell

POWER (typ.)	Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® U3405 (ULV) 1.07 GHz
5 V	13 W	19.5 W	29.5 W	12 W
3.3 V	4.5 W	4.5 W	4.5 W	4.5 W
Total	17.5 W	24 W	34 W	16.5 W

Table 5-5: CP3002 with Win. XP and Processor and Graphics in Idle State

POWER (typ.)	Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® U3405 (ULV) 1.07 GHz
5 V	6 W	6 W	6 W	6 W
3.3 V	4.5 W	4.5 W	4.5 W	4.5 W
Total	10.5 W	10.5 W	10.5 W	10.5 W

Table 5-6: CP3002 with Win. XP and Max. Proc. Workload and Graphics in Idle State

POWER (typ.)	Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® U3405 (ULV) 1.07 GHz
5 V	15 W	23 W	34 W	14 W
3.3 V	5 W	5 W	5 W	5 W
Total	20 W	28 W	39 W	19 W

Table 5-7: CP3002 with Win. XP and Max. Processor and Graphics Workload

POWER (typ.)	Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® U3405 (ULV) 1.07 GHz
5 V	17 W	28 W	38 W	16 W
3.3 V	8 W	8 W	9 W	8 W
Total	25 W	36 W	47 W	24 W

5.3 Power Consumption of CP3002 Accessories

The following table indicates the power consumption of the CP3002 accessories.

Table 5-8: Power Consumption of CP3002 Accessories

MODULE	POWER 5 V	POWER 3.3 V
DDR3 SDRAM update from 4 GB to 8 GB	—	approx. 1 W
SATA Flash module	—	approx. 0.5 W
Gigabit Ethernet (per interface)	approx. 0.7 W	—

5.4 Start-Up Currents of the CP3002

The following table indicates the basic start-up currents of the CP3002 during the first 2-3 seconds after the power supply has been switched on.

Table 5-9: Start-Up Currents of the CP3002

POWER		Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® U3405 (ULV) 1.07 GHz
5 V	peak	7.5 A	7.5 A	7.5 A	7.5 A
3.3 V	peak	5 A	5 A	5 A	5 A

For further information on the start-up current, please contact Kontron.

Chapter 6

Thermal Considerations

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6. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing CP3002 applications.

6.1 Board Internal Thermal Monitoring

To ensure optimal operation and long-term reliability of the CP3002, all onboard components must remain within the maximum temperature specifications. The most critical component on the CP3002 is the processor. Operating the CP3002 above the maximum operating limits will result in permanent damage to the board.

The board includes three integrated temperature sensors to measure the processor and the chipset temperature:

- Two thermal sensors integrated in the processor
- One thermal sensor integrated in the chipset

6.2 Processor Thermal Monitoring

To allow optimal operation and long-term reliability of the CP3002, the Intel® processor must remain within the maximum die temperature specifications. The maximum die temperature for the Intel® multi-chip package processors is as follows:

- Processor die: 105°C
- Graphics and memory controller die: 100°C

The Intel® processor uses the Adaptive Thermal Monitor feature to protect the processor from overheating and includes the following on-die temperature sensors:

- Two Digital Thermal Sensors (DTS) for the processor cores
- One Digital Thermal Sensor (DTS) for the graphics controller and the memory controller
- Catastrophic Cooling Failure Sensor (THERMTRIP#)

These sensors are integrated in the processor and work without any interoperability of the uEFI BIOS or the software application. Enabling the Thermal Control Circuit in the uEFI BIOS allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

6.2.1 Digital Thermal Sensor (DTS)

The Intel® processor includes three on-die Digital Thermal Sensors (DTS), two for the processor cores and one for the graphics controller and the memory controller. They can be read via an internal register of the processor. The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating temperature. Via the Digital Thermal Sensors, the uEFI BIOS or the application software can measure the processor die temperature.

6.2.2 Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature reduces the processor power consumption and the temperature when the processor silicon exceeds the Thermal Control Circuit (TCC) activation temperature until the processor operates at or below its maximum operating temperature. The temperature at which the Adaptive Thermal Monitor activates the Thermal Control Circuit is not user-configurable.

The processor core power reduction is achieved by:

- Frequency/VID Control (by reducing of processor core voltage)
- Clock Modulation (by turning the internal processor core clocks off and on)

Adaptive Thermal Monitor dynamically selects the appropriate method. uEFI BIOS is not required to select a specific method as with previous-generation processors supporting Intel® Thermal Monitor 1 (TM1) and Intel® Thermal Monitor 2 (TM2).

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

6.2.3 Frequency/VID Control

Frequency/VID Control reduces the processor's operating frequency (using the core ratio multiplier) and the input voltage (using VID signals). This combination of lower frequency and VID results in a reduction of the processor power consumption. This method is similar to Intel® Thermal Monitor 2 (TM2) in previous generation processors.

Running the processor at the lower frequency and voltage will reduce power consumption and should allow the processor to cool off. If the processor temperature does not drop below the TCC activation point, a second frequency and voltage transition will take place. This sequence of temperature checking and Frequency/VID reduction will continue until either the minimum frequency has been reached or the processor temperature has dropped below the TCC activation point. If the processor temperature remains above the TCC activation point even after the minimum frequency has been reached, then Clock Modulation at that minimum frequency will be initiated.

Note ...

When the TH LED on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 105 °C or the graphics and memory controller die temperature is above 100 °C.

6.2.4 Clock Modulation

Clock Modulation reduces power consumption by rapidly turning the internal processor core clocks off and on at a duty cycle that should reduce power dissipation (typically a 30-50% duty cycle). This method is similar to Intel® Thermal Monitor 1 (TM1) in previous generation processors.

Once the temperature has dropped below the maximum operating temperature, the TCC goes inactive and clock modulation ceases.

Note ...

When the TH LED on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 105 °C or the graphics and memory controller die temperature is above 100 °C.

6.2.5 Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating. The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 125 °C. Once activated, the event remains latched until the CP3002 undergoes a power-on restart (all power off and then on again).

This function cannot be enabled or disabled in the uEFI BIOS. It is always enabled to ensure that the processor is protected in any event.

Note ...

When the TH LED on the front panel is blinking red at regular intervals, it indicates that the processor temperature is above 125 °C.

6.3 Chipset Thermal Monitor Feature

The Intel® QM57 chipset includes one on-die thermal sensor to measure the chipset die temperature.

The maximum Intel® QM57 chipset case temperature is 111 °C.

6.4 External Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the CP3002 is equipped with a heat sink. Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed. The physical size, shape, and construction of the heat sink ensures the lowest possible thermal resistance. In addition, the CP3002 has been specifically designed to efficiently support forced airflow as found in modern CompactPCI systems.

Thermal Characteristic Graphs

The thermal characteristic graphs shown on the following sections illustrate the maximum ambient air temperature as a function of the volumetric airflow rate for the power consumption indicated. The diagrams are intended to serve as guidance for reconciling board and system with the required computing power considering the thermal aspect. One diagram per CPU version level is provided. There are up to two curves representing upper level working points based on different levels of average CPU utilization. When operating below the corresponding curve, the CPU runs steadily without any intervention of thermal supervision. When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop in order to protect the CPU and the chipset from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

An airflow of 2.0 m/s is a typical value for a standard *Kontron* ASM rack. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient operating temperature, the processor and chipset junction temperature must never exceed the specified limit for the involved processor and chipset.

Thermal characteristic curves

- Thermal characteristic curve of the CP3002 with maximum processor workload and graphics controller off or idle
  This load complies with the values indicated in Table 5-6, Chapter 5.2, “Power Consumption”.
- Thermal characteristic curve of the CP3002 with maximum processor and graphics controller workload
  This load complies with the values indicated in Table 5-7, Chapter 5.2, “Power Consumption”.

How to read the diagram

Select a specific CPU and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must be more than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth. The volumetric flow rate is specified in m^3/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m^3/h; 1 m^3/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s (meter-per-second) or in fps (feet-per-second) respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps

The following figures illustrate the operational limits of the CP3002 taking into consideration power consumption vs. ambient air temperature vs. airflow rate. The measurements were made based on a 4HP slot and with both processor cores enabled.

6.4.1 Operational Limits for the CP3002

Figure 6-1: CP3002 with i7-660UE, 1.33 GHz

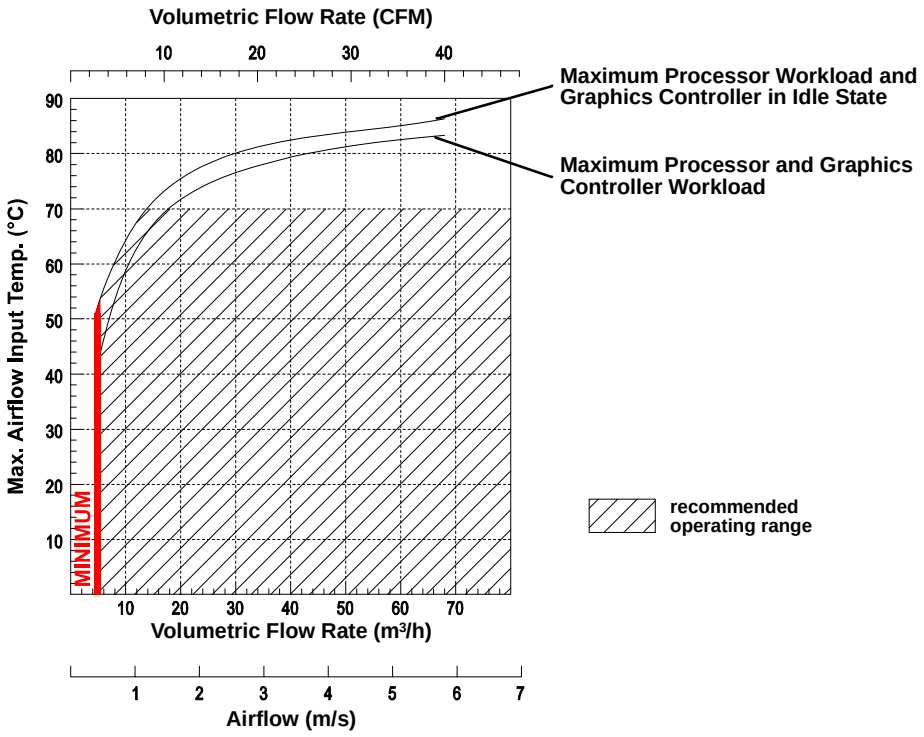


Figure 6-2: CP3002 with i7-620LE, 2.0 GHz

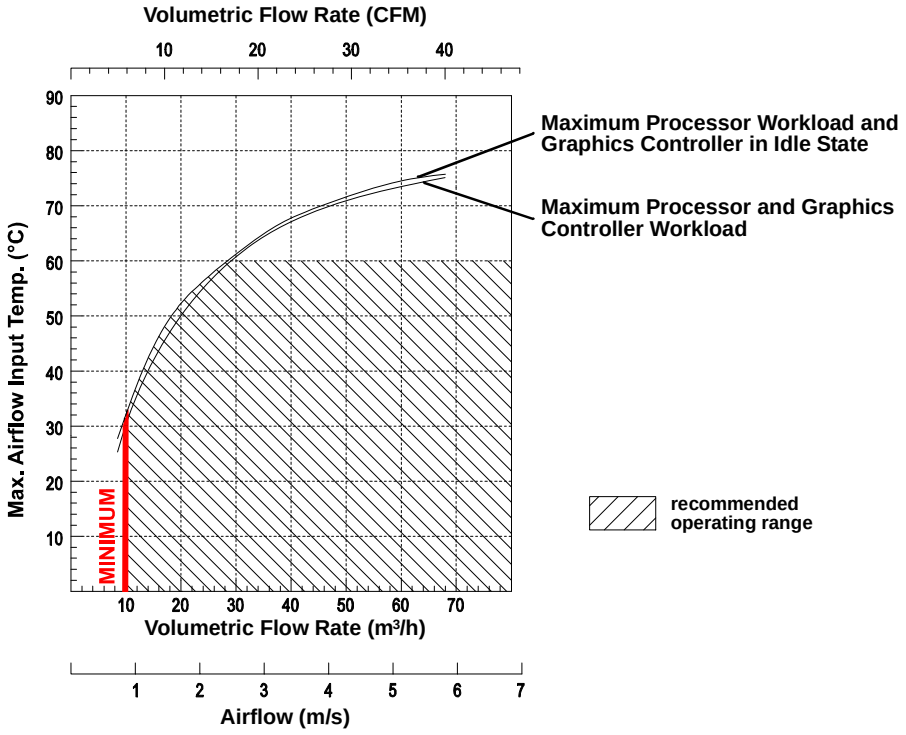


Figure 6-3: CP3002 with i7-610E, 2.53 GHz

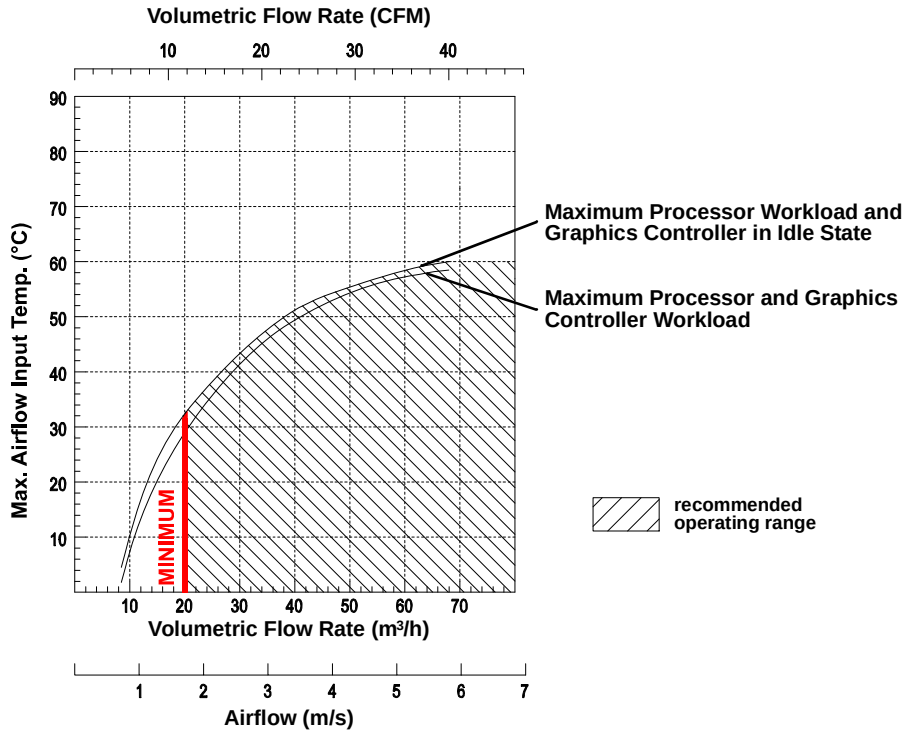
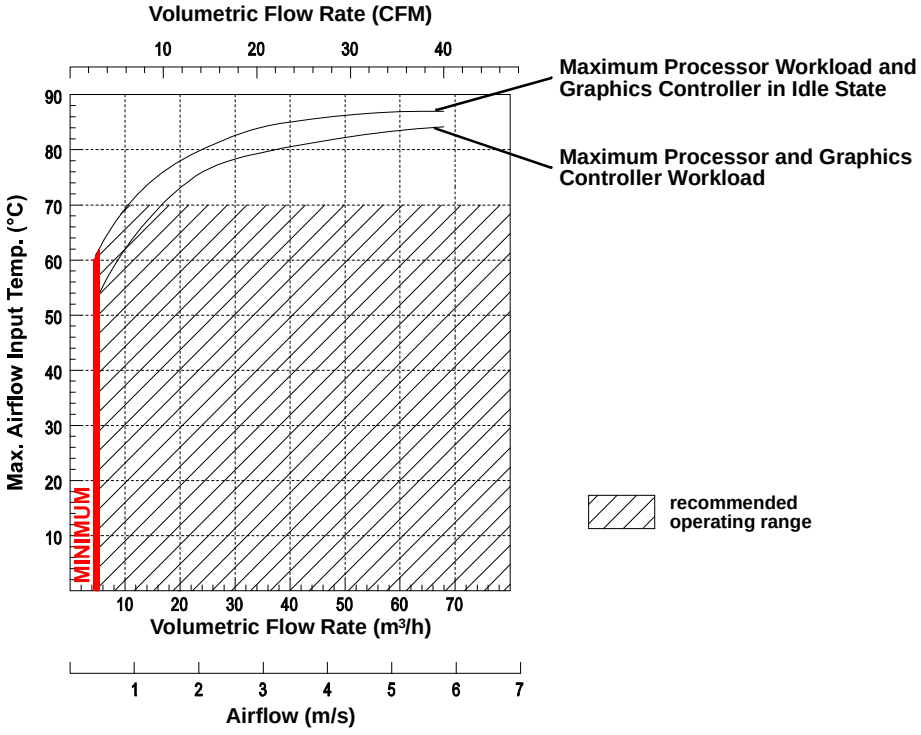


Figure 6-4: CP3002 with Celeron® U3405, 1.07 GHz



6.4.2 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the CP3002 must also be considered. Devices such as SATA Flash modules which are directly attached to the CP3002 must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

Warning!

As Kontron assumes no responsibility for any damage to the CP3002 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP3002 complies with the thermal considerations set forth in this document.

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Chapter A

CP3002-HDD

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A. CP3002-HDD Module

A.1 Overview

The CP3002-HDD module has been designed to include a COM port, a SATA drive (HDD/SSD) interface, two USB 2.0 interfaces, a CFast card socket, a DVI-D flat panel interface, and a battery socket. The CP3002-HDD module expands the CP3002 board from 4HP to 8HP. This additional capability opens up the broadest range of expansion possibilities.

The connectors for the COM port, the USB ports, and the DVI-D port are situated at the front panel, while the SATA connector, the CFast card socket are onboard connectors. The module connects to the CP3002 via the high-speed I/O extension connector.

The battery socket on the CP3002-HDD module has the same function as the battery socket on the CP3002.

Note ...

If a CP3002-HDD module is used on the CP3002, either the CP3002 or the CP3002-HDD module may be equipped with a battery.

Using one battery on the CP3002 and one on the CP3002-HDD module simultaneously may result in premature discharge of the batteries.

Note ...

If the CP3002-HDD module is mounted on the CP3002, the SATA Flash module cannot be used on the CP3002.

Either the CP3002-HDD module or the SATA Flash module can be mounted on the CP3002.

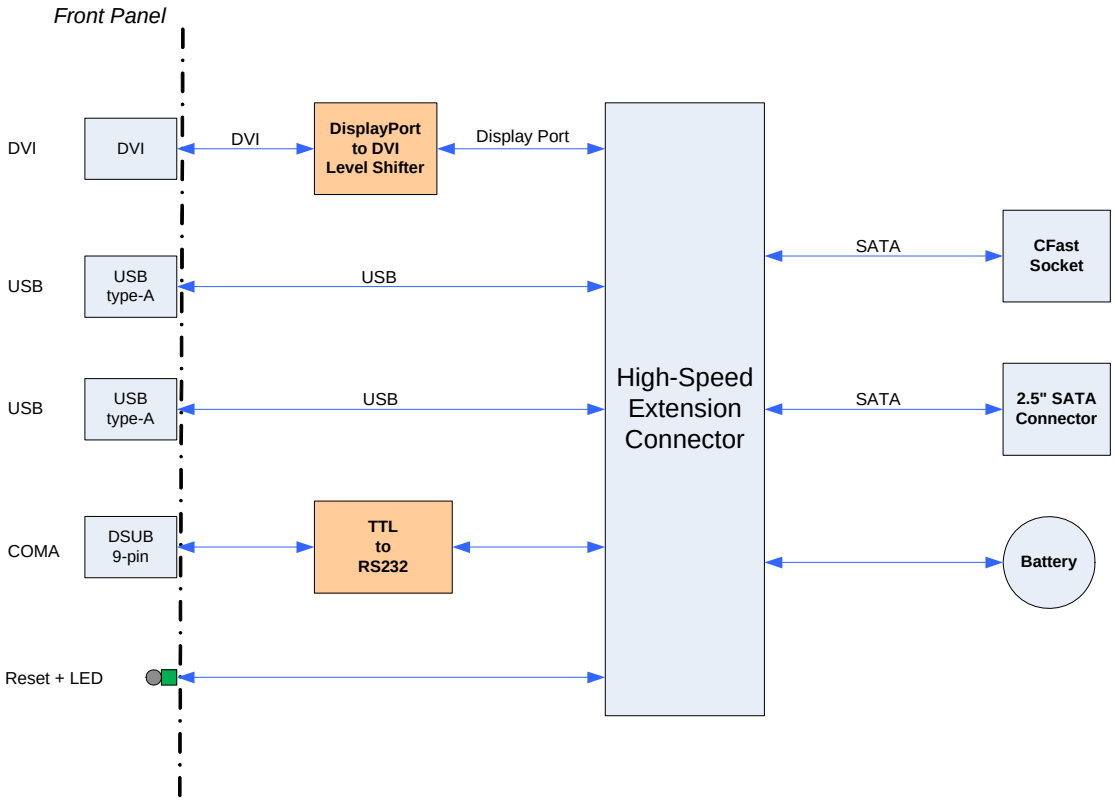
A.2 Technical Specifications

Table A-1: CP3002-HDD Module Specifications

CP3002-HDD		SPECIFICATIONS
Front Panel Interfaces	Serial Port	One 16C550-compatible serial port (COMA), RS-232; 9-pin D-Sub connector; J5
	USB	Two USB 2.0 connectors, J2 and J4
	DVI-D	One DVI-D connector with digital signals only, J1
Onboard Interfaces	SATA	SATA connector, J3, for connecting a SATA 2.5” HDD/SSD
	CFast	One CFast card socket, J6
	Board-to-Board	One high-speed I/O extension connector, J7, for connecting the module to the CP3002
Indicators/ Switches	HDD LED	One LED (green) monitors SATA activity
	Front Panel Switch	Reset button, guarded
General	Power Consumption	Power consumption without hard disk, CFast card and peripheral devices connected: 100 mA at 3.3 V
	Temperature Range	Operational: 0°C to +60°C Standard Storage: -55°C to +85°C Without hard disk and without battery -40°C to +65°C With hard disk  *Note ...* When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP3002-HDD module (See "Battery" below).
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	Dimensions: 100 mm x 158 mm
	Board Weight	482 grams (8 HP CP3002 with CP3002-HDD, heat sink, front panel, two 2 GB SODIMM memory modules and battery, but without CFast card and 2.5” HDD/SSD)
	Battery	3.0V lithium battery for RTC with battery socket. Recommended type: CR2025 Temperature ranges: Operational: -20°C to +70°C typical (refer to the battery manufacturer’s specifications for exact range) Storage: -55°C to +70°C typical (no discharge)

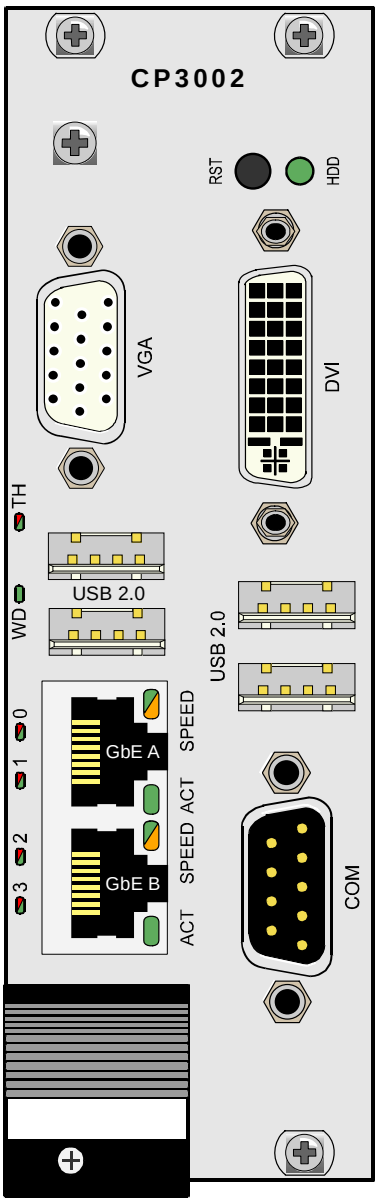
A.3 CP3002-HDD Module Functional Block Diagram

Figure A-1: CP3002-HDD Module Functional Block Diagram



A.4 Front Panel of the 8HP CP3002 with CP3002-HDD Module

Figure A-2: Front Panel of the 8HP CP3002 with CP3002-HDD Module



Watchdog and Overtemperature Status LEDs:

WD (green):	Watchdog Status
TH (red/green):	Overtemperature Status

SATA LED:

HDD (green):	Monitors SATA Activity

General Purpose LEDs:

LED0..3 (red/green/red+green):	General Purpose/POST Code

Note ...

If the General Purpose LEDs 0..3 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started.

For further information, please contact Kontron.

Ethernet LEDs:

ACT (green):	Ethernet Link/Activity
SPEED (green/orange):	Ethernet Speed

A.5 CP3002-HDD Module Layout

Figure A-3: CP3002-HDD Module Layout (Top View)

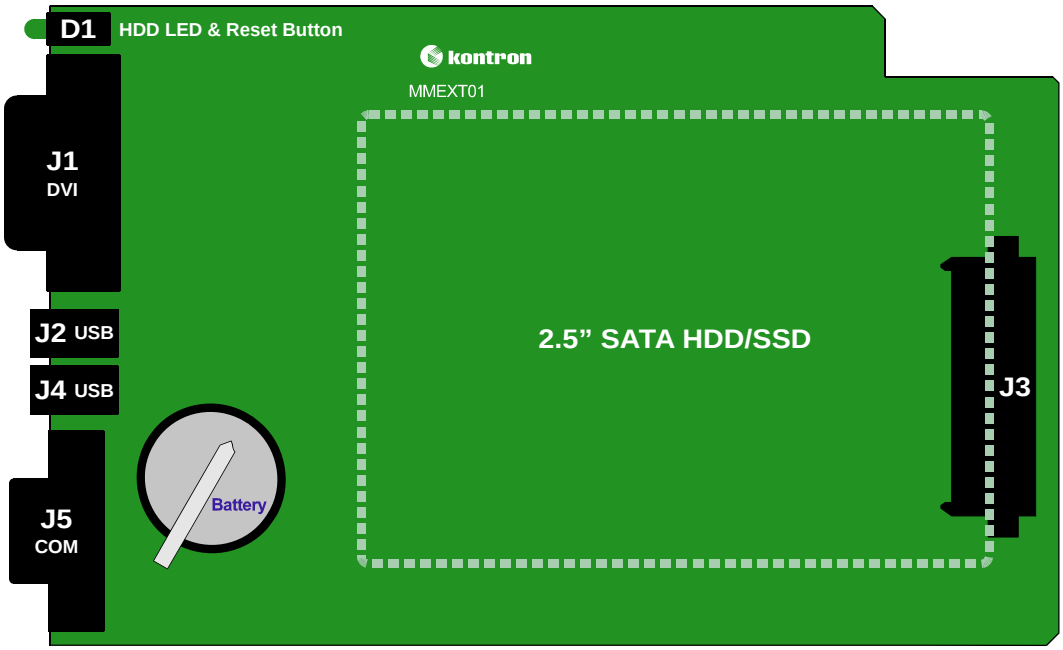
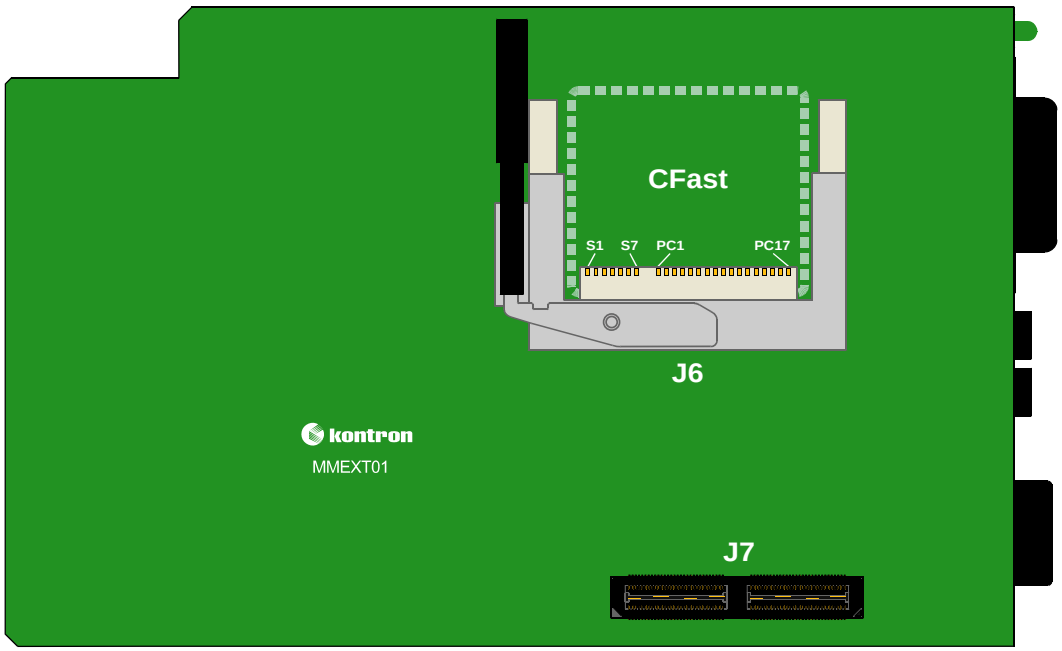


Figure A-4: CP3002-HDD Module Layout (Bottom View)



A.6 Module Interfaces (Front Panel and Onboard)

A.6.1 Serial Port

One PC-compatible, serial RS-232, 9-pin D-Sub port is available, which is fully compatible with the 16C550 controller. This port includes a complete set of handshaking and modem control signals. Data transfer rates up to 115.2 kB/s are supported.

The COMA interface is routed to the serial port connector J5.

Figure A-5: Serial Port Connector J5

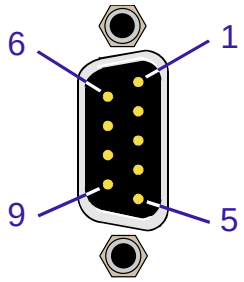


Table A-2: Serial Port Connector J5 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	DCD	Data carrier detect	I
2	RXD	Receive data	I
3	TXD	Transmit data	O
4	DTR	Data terminal ready	O
5	GND	Signal ground	--
6	DSR	Data send request	I
7	RTS	Request to send	O
8	CTS	Clear to send	I
9	RI	Ring indicator	I

A.6.2 USB Interfaces

The CP3002-HDD provides two standard USB 2.0 ports on J2 and J4. The USB 2.0 ports are high-speed, full-speed, and low-speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s.

One USB peripheral may be connected to each port. To connect more USB devices than there are available ports, an external hub is required.

Figure A-6: USB Connectors J2 and J4

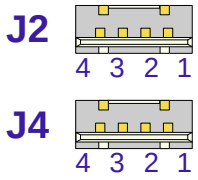


Table A-3: USB Connectors J2 and J4 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	O
2	USB-	Differential USB-	I/O
3	USB+	Differential USB+	I/O
4	GND	GND	--

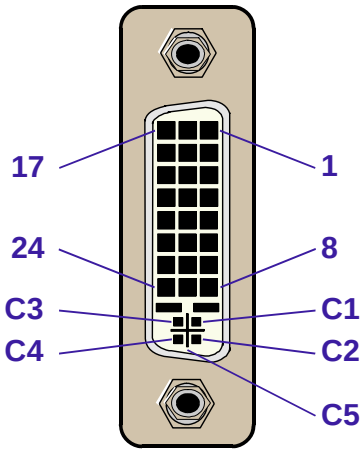
Note ...

The CP3002-HDD host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

A.6.3 DVI-D Interface

The CP3002-HDD provides one standard DVI-D interface, J1, which is a digital signal only interface with device detection.

Figure A-7: DVI-D Connector J1



The following table indicates the pinout of the DVI-D Connector J1.

Table A-4: DVI-D Connector J1 Pinout

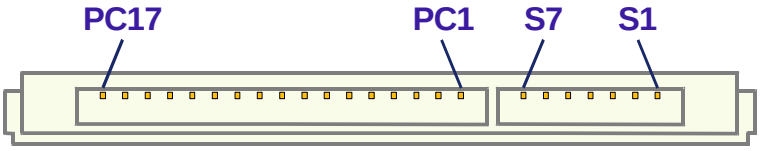
PIN	SIGNAL	DESCRIPTION	I/O	PIN	SIGNAL	DESCRIPTION	I/O
1	TMDS Data 2-	TMDS* Link -	O	13	NC	Not connected	--
2	TMDS Data 2+	TMDS Link +	O	14	VCC	Power +5 V, 0.5A fused	--
3	GND	Ground	--	15	GND	Ground	--
4	NC	Not connected	--	16	HPDETECT	Hot Plug Detect	I
5	NC	Not connected	--	17	TMDS Data 0-	TMDS Link -	O
6	DDC Clock	I^2C™ Clock	O	18	TMDS Data 0+	TMDS Link +	O
7	DDC Data	I^2C™ Data	I/O	19	GND	Ground	--
8	NC	Not connected	--	20	NC	Not connected	--
9	TMDS Data 1-	TMDS Link -	O	21	NC	Not connected	--
10	TMDS Data 1+	TMDS Link +	O	22	GND	Ground	--
11	GND	Ground	--	23	TMDS Clock +	TMDS Link +	O
12	NC	Not connected	--	24	TMDS Clock -	TMDS Link -	O
C1	NC	Not connected	--	C4	NC	Not connected	--
C2	NC	Not connected	--	C5	GND	Ground	--
C3	NC	Not connected	--				

* TMDS = Transition Minimized Differential Signaling

A.6.4 CFast Card Connector

To enable flexible flash expansion, a CFast card connector, J6, is available on the CP3002-HDD.

Figure A-8: CFast Connector J6



The following table provides the pinout for the CFast connector J6.

Table A-5: CFast Connector J6 Pinout

PIN		SIGNAL	FUNCTION	I/O
Signal Segment	S1	GND	Ground signal	--
	S2	SATA_TX+	Differential Transmit+	O
	S3	SATA_TX-	Differential Transmit-	O
	S4	GND	Ground signal	--
	S5	SATA_RX-	Differential Receive-	I
	S6	SATA_RX+	Differential Receive+	I
	S7	GND	Ground signal	--
Power Segment	PC1	RSV	Reserved	--
	PC2	GND	Ground signal	--
	PC3	NC	Not connected	--
	PC4	NC	Not connected	--
	PC5	NC	Not connected	--
	PC6	NC	Not connected	--
	PC7	GND	Ground signal	--
	PC8	RSV	Reserved	--
	PC9	RSV	Reserved	--
	PC10	NC	Not connected	--
	PC11	NC	Not connected	--
	PC12	NC	Not connected	--
	PC13	3.3V	3.3V power	--
	PC14	3.3V	3.3V power	--
	PC15	GND	Ground signal	--
	PC16	GND	Ground signal	--
	PC17	RSV	Reserved	--

A.6.5 SATA Interface

The SATA connector, J3, on the CP3002-HDD module is provided for connecting a 2.5” SATA HDD/SSD to the CP3002-HDD module and is divided into three segments: a primary signal segment, a secondary signal segment, and a power segment.

Figure A-9: SATA Connector J3

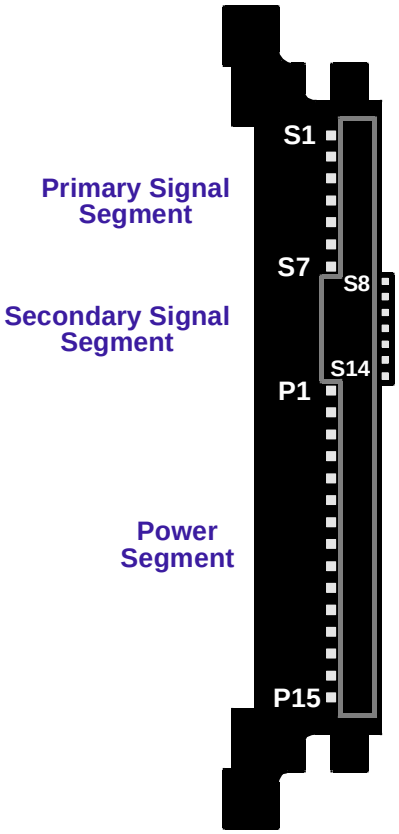


Table A-6: SATA Connector J3 Pinout

PIN		SIGNAL	FUNCTION	I/O
Primary Signal Segment	S1	GND	Ground signal	--
	S2	SATA_TX+	Differential Transmit+	O
	S3	SATA_TX-	Differential Transmit-	O
	S4	GND	Ground signal	--
	S5	SATA_RX-	Differential Receive-	I
	S6	SATA_RX+	Differential Receive+	I
	S7	GND	Ground signal	--
Secondary Signal Segment	S8	GND	Ground signal	--
	S9	NC	Not connected	--
	S10	NC	Not connected	--
	S11	GND	Ground signal	--
	S12	NC	Not connected	--
	S13	NC	Not connected	--
	S14	GND	Ground signal	--
Power Segment	P1	3.3V	3.3V power	--
	P2	3.3V	3.3V power	--
	P3	3.3V	3.3V power	--
	P4	GND	Ground signal	--
	P5	GND	Ground signal	--
	P6	GND	Ground signal	--
	P7	5V	5V power	--
	P8	5V	5V power	--
	P9	5V	5V power	--
	P10	GND	Ground signal	--
	P11	RES	Reserved	--
	P12	GND	Ground signal	--
	P13	NC (12V)	Not connected	--
	P14	NC (12V)	Not connected	--
	P15	NC (12V)	Not connected	--

A.6.6 Battery

The CP3002-HDD may be equipped with a 3.0 V “coin cell” lithium battery for the RTC on the CP3002.

Note ...

If an CP3002-HDD module is used on the CP3002, either the CP3002 or the CP3002-HDD module may be equipped with a battery.

Using one battery on the CP3002 and one on the CP3002-HDD module simultaneously may result in premature discharge of the batteries.

To replace the battery, proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery type is CR2025.

Note ...

The user must be aware that the battery’s operational temperature range is less than the CP3002-HDD’s storage temperature range.

For exact range information, refer to the battery manufacturer’s specifications.

Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer’s instructions.

The typical life expectancy of a 170 mAh battery (CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.

To ensure that the lifetime of the battery has not been exceeded, it is recommended to exchange the battery after 4 - 5 years.

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Appendix B

CP-RIO3-04

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B. CP-RIO3-04 Rear I/O Module

B.1 Overview

The CP3002 provides optional rear I/O connectivity for peripherals, a feature which may be particularly useful in specialized CompactPCI systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connector J2 on the CP3002.

When the CP-RIO3-04 rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface.

To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. The CP3002 with rear I/O is compatible with all standard CompactPCI passive backplanes with rear I/O support.

The CP-RIO3-04 rear I/O module provides the following interfaces.

- CompactPCI rear I/O
- Two USB 2.0 ports
- Two Gigabit Ethernet ports without LED signals
- Two COM ports
- VGA analog port
- Two SATA ports
- Power supply management

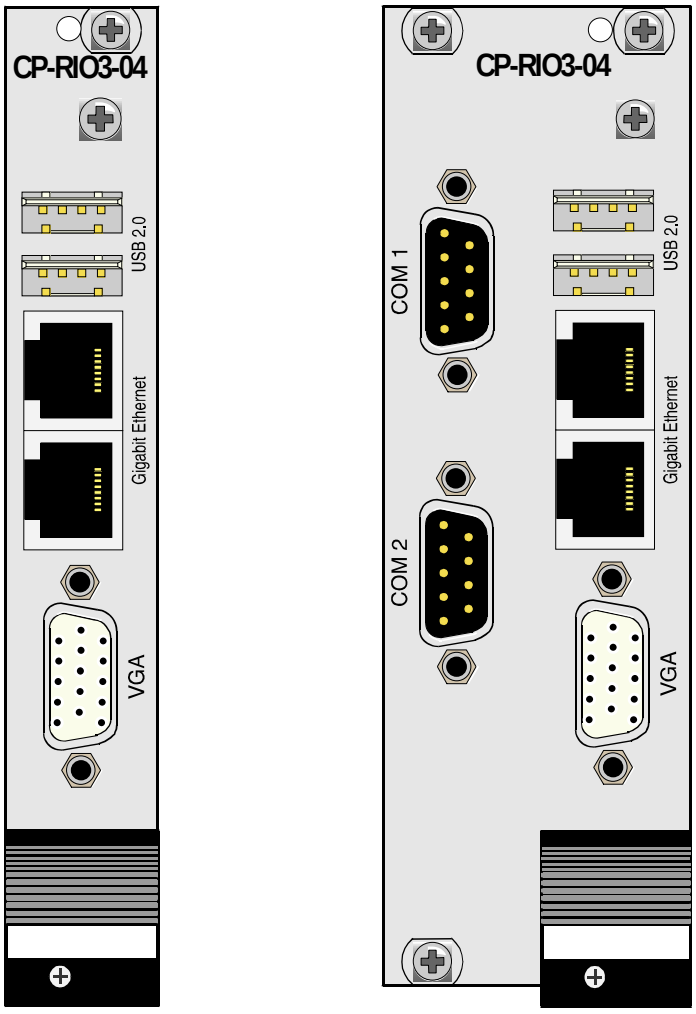
B.2 Technical Specifications

Table B-1: CP-RIO3-04 Rear I/O Module Main Specifications

CP-RIO3-04		SPECIFICATIONS
External Interfaces	USB	Two USB 2.0 interfaces; two 4-pin connectors
	VGA	One VGA interface; 15-pin D-Sub connector
	Ethernet	Two Gigabit Ethernet interfaces implemented as dual RJ-45 connector without LEDs
	COM	Two onboard, RS-232 serial ports with full modem support, COMA (COM1) and COMB (COM2) On the 8HP version, the serial ports are routed to the front panel and implemented as two 9-pin D-Sub connectors.
Internal Interfaces	SATA	Two SATA interfaces implemented as two 7-pin, L-form standard SATA connectors
	Peripheral Control	One 10-pin, 2.54 mm onboard connector for power supply management
	Compact PCI	CompactPCI connector for connecting rear I/O to the backplane
	COM	Two COM ports implemented as two 10-pin, 2.54 mm onboard connectors (4HP only) full modem support
General	Temperature Range	Operational: 0°C to +60°C Storage: -55°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 80 mm
	Board Weight	4HP: 120 grams 8HP: 150 grams

B.3 Front Panels

Figure B-1: CP-RIO3-04 Front Panels, 4HP and 8HP Versions



4 HP 8 HP

B.4 Module Layout: 4HP and 8HP Versions

Figure B-2: CP-RIO3-04 Rear I/O Module Layout, 4HP Version

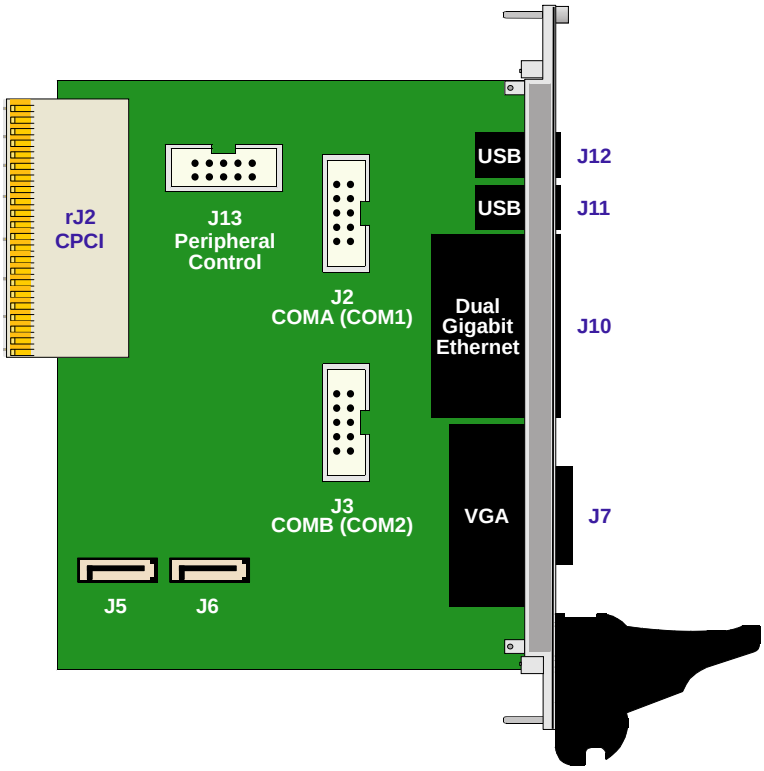
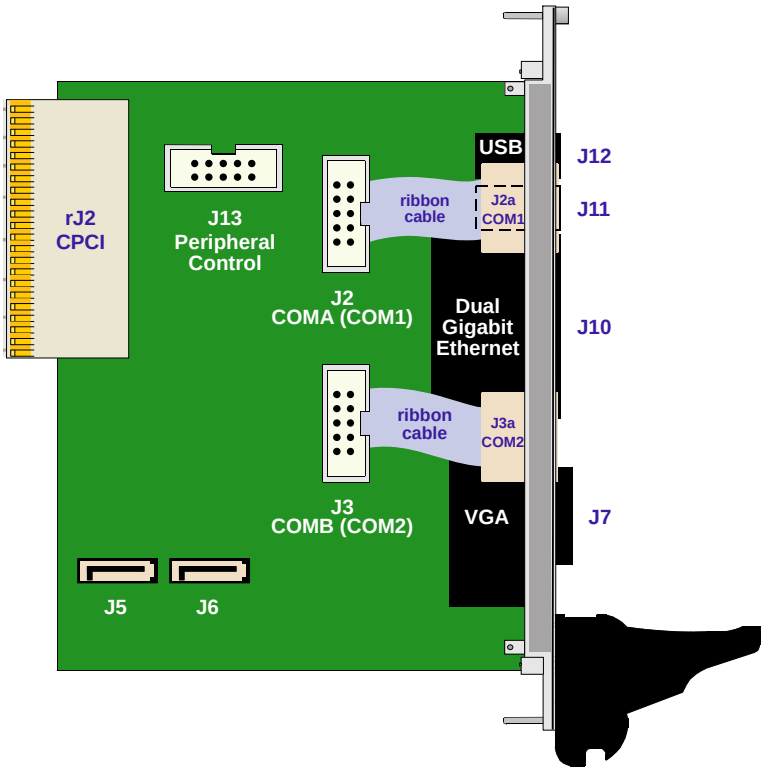


Figure B-3: CP-RIO3-04 Rear I/O Module Layout, 8HP Version



B.5 Module Interfaces

B.5.1 USB Interfaces

There are two identical USB interfaces on the CP-RIO3-04 rear I/O module, each with a maximum transfer rate of 480 Mb/s provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more USB devices than there are available ports, an external hub is required.

Figure B-4: USB Con. J11/J12

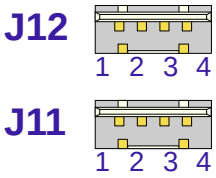


Table B-2: USB Con. J11 and J12 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	VCC	VCC signal	O
2	USB-	Differential USB-	I/O
3	USB+	Differential USB+	I/O
4	GND	GND signal	--

Note ...

The USB host interfaces on the CP-RIO3-04 rear I/O module can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

Note ...

The rear I/O interface supports the USB 1.1 and USB 2.0 standards. For USB 2.0 it is strongly recommended to use a cable length not exceeding 3 meters.

B.5.2 VGA Interface

The 15-pin female connector J7 is used to connect a VGA monitor to the CP-RIO3-04 rear I/O module.

Figure B-5: D-Sub VGA Connector J7

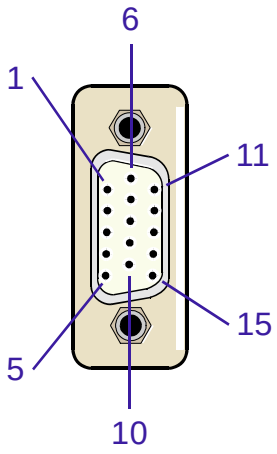


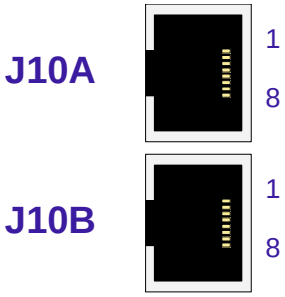
Table B-3: D-Sub VGA Connector J7 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	Red	Red video signal output	O
2	Green	Green video signal output	O
3	Blue	Blue video signal output	O
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I^2C data	I/O
15	Sclk	I^2C clock	O
9	VCC	Power +5V, 140 mA fuse protection	O
5,6,7,8, 10	GND	Ground signal	--
4,11	NC	--	--

B.5.3 Gigabit Ethernet Interface

The Ethernet connectors are realized as RJ-45 connectors. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Figure B-6: Dual Gigabit Ethernet Connector J10A/B



RJ-45 Connector J10A/B Pinout

The J10A/B connector supplies the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller.

Table B-4: Dual Gigabit Ethernet Connector J10A/B Pinout

PIN	MDI / STANDARD ETHERNET CABLE					
	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-

Note ...

The Ethernet transmission can operate effectively with structured cable that meets CAT5 cable or higher specifications.

B.5.4 COM Interface

The CP-RIO3-04 rear I/O module provides two identical COM ports for connecting RS-232 devices to the CP-RIO3-04 rear I/O module.

On the 8HP version, the onboard 10-pin COM connectors J2 and J3 are routed to the 9-pin D-Sub COM connectors J2a and J3a located on the front panel.

On the 4HP version, the COM signals are available only on the onboard 10-pin COM connectors J2 and J3.

The following figure and table provide pinout information for the 9-pin D-Sub COM connectors J2a and J3a located on the front panel of the 8HP version.

Figure B-7: COM Connectors J2a (COMA) and J3a (COMB)

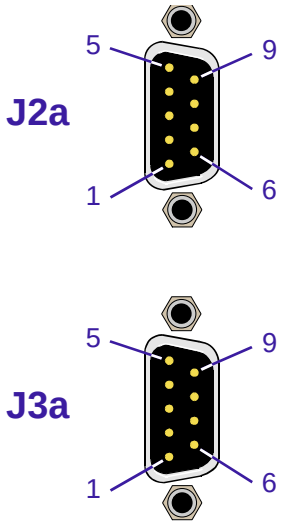


Table B-5: COM Connectors J2a (COMA) and J3a (COMB) Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	DCD	Data carrier detect	I
2	RXD	Receive data	I
3	TXD	Transmit data	O
4	DTR	Data terminal ready	O
5	GND	Signal ground	--
6	DSR	Data send request	I
7	RTS	Request to send	O
8	CTS	Clear to send	I
9	RI	Ring indicator	I

The following figure and table provide pinout information for the onboard serial port connectors J2 and J3.

Figure B-8: Serial Port Connectors J2 (COMA) and J3 (COMB)

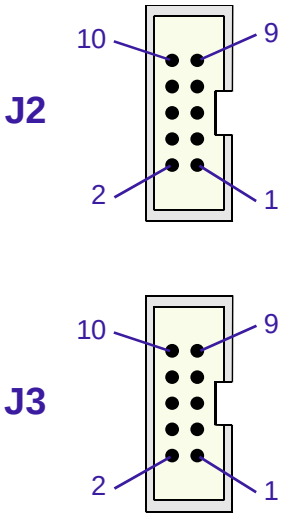


Table B-6: Serial Port Con. J2 (COMA) and J3 (COMB) Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	DCD	Data carrier detect	I
2	DSR	Data send request	I
3	RXD	Receive data	I
4	RTS	Request to send	O
5	TXD	Transmit data	O
6	CTS	Clear to send	I
7	DTR	Data terminal ready	O
8	RI	Ring indicator	I
9	GND	Signal ground	--
10	NC	Not connected	--

B.5.5 Peripheral Control Interface

A power supply with power management can be connected to the CP-RIO3-04 via the peripheral control connector J13.

The following figure and table provide pinout information for connector J13.

Figure B-9: Peripheral Con. J13

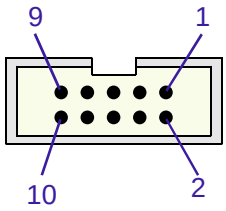


Table B-7: Peripheral Connector J13 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	GND	Signal ground	--
2	PWR_5VSTDBY	+5V standby power (optional)	I
3	RSV	Reserved	--
4	VCC5V	Power +5V	O
5	RSV	Reserved	--
6	VCC3V3	Power +3.3V	O
7	PWR_SLPS3#	Power supply sleep mode	O
8	GND	Signal ground	--
9	PWR_BTN#	Wake-up / sleep input	I
10	GND	Signal ground	--

B.5.6 Serial ATA Interfaces

The onboard Serial ATA connectors J5 and J6 allow the connection of standard HDDs and other Serial ATA devices to the CP-RIO3-04 rear I/O module.

The following figure and table provide pinout information for the SATA connectors J5 and J6.

Figure B-10: SATA Con. J5 and J6

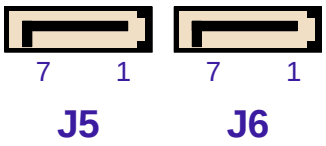


Table B-8: SATA Connectors J5 and J6 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	GND	Ground signal	--
2	SATA_TX+	Differential Transmit +	O
3	SATA_TX-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX-	Differential Receive -	I
6	SATA_RX+	Differential Receive +	I
7	GND	Ground signal	--

Note ...

When using a Serial ATA cable, it is recommended to use a special right-angled Serial ATA cable due to possible space limitations within the system. For further information, please contact Kontron.

B.5.7 Rear I/O Interface on CompactPCI Connector rJ2

The CP-RIO3-04 rear I/O module conducts a wide range of I/O signals through the rear I/O connector rJ2.

Warning!

To support the rear I/O feature, a 3U CompactPCI backplane with rear I/O support is required. Do not plug a rear I/O configured board in a backplane without rear I/O support. Failure to comply with the above will result in damage to your board.

Figure B-11: Rear I/O CompactPCI Connector rJ2

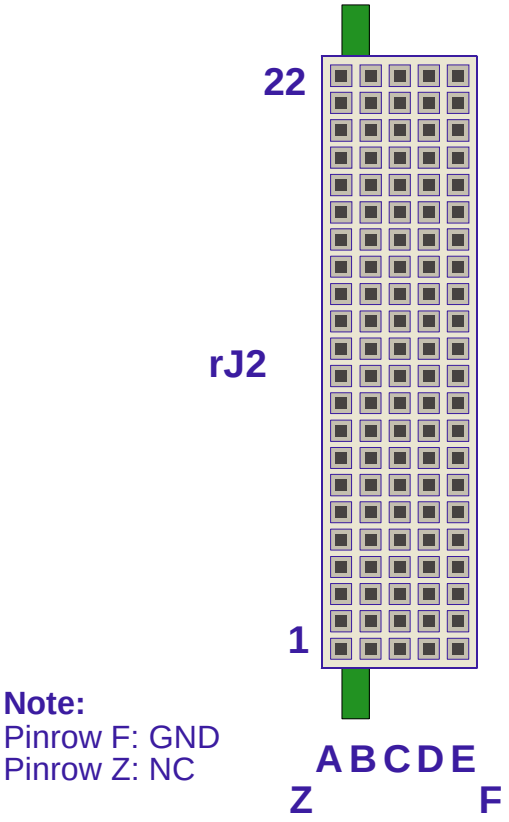


Table B-9: Rear I/O CompactPCI Connector rJ2 Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	NC	NC	NC	NC	NC	NC	GND
21	NC	NC	GND	USBA+ / bi	USBB+ / bi	USBA_PWR_5V / in	GND
20	NC	NC	GND	USBA- / bi	USBB- / bi	USBB_PWR_5V / in	GND
19	NC	GND	GND	PWR_BTN# / out	PWR_SLPS3# / in	RIO_3.3V / in	GND
18	NC	COMA_RXD / out	COMA_DCD# / out	COMA_DTR# / in	COMB_CTS# / out	COMA_CTS# / out	GND
17	NC	COMA_TXD / in	COMB_RXD / out	NC	NC	NC	GND
16	NC	COMA_DSR# / out	COMA_RTS# / in	NC	RSV	COMA_RI# / out	GND
15	NC	PWR_5VSTDBY / out	RSV	NC	NC	NC	GND
14	NC	IPA_DA+ / bi	IPA_DA- / bi	COMB_RTS# / in	IPA_DC+ / bi	IPA_DC- / bi	GND
13	NC	IPA_DB+ / bi	IPA_DB- / bi	COMB_RI# / out	IPA_DD+ / bi	IPA_DD- / bi	GND
12	NC	IPB_DA+ / bi	IPB_DA- / bi	RIO_1V9 / in	IPB_DC+ / bi	IPB_DC- / bi	GND
11	NC	IPB_DB+ / bi	IPB_DB- / bi	COMB_DCD# / out	IPB_DD+ / bi	IPB_DD- / bi	GND
10	NC	GND	COMB_TXD / in	VGA_RED / in	COMB_DTR# / in	GND	GND
9	NC	SATAATX+ / in	GND	VGA_HSYNC / in	GND	SATABTX+ / in	GND
8	NC	SATAATX- / in	GND	VGA_BLUE / in	GND	SATABTX- / in	GND
7	NC	GND	COMB_DSR# / out	VGA_DDC_DATA / bi	RSV	GND	GND
6	NC	SATAARX+ / out	GND	VGA_GREEN / in	GND	SATABRX+ / out	GND
5	NC	SATAARX- / out	GND	VGA_VSYNC / in	GND	SATABRX- / out	GND
4	NC	NC	RIO_5V / in	VGA_DDC_CLK / in	GPIO_CFG0 / out	GND	GND
3	NC	NC	GND	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	NC	GND
1	NC	NC	NC	NC	NC	NC	GND

Warning!

The RIO_XXX signals are power supply **INPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Table B-10: Rear I/O Signal Description

SIGNAL	DESCRIPTION
COMAx	COMA port LVTTL (3.3V)
COMBx	COMB port LVTTL (3.3V)
GPIO_CFG0	COMB configuration
IPx	Gigabit Ethernet copper port
SATAx	Serial ATA port
USBx	USB interface and power
VGAx	VGA signal
RIOx	Power supply signal
PWRx	Power management signal
RSV	Reserved
GND	Ground signal
NC	Not connected

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Appendix C

SATA Flash Module

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C. SATA Flash Module

The 4HP CP3002 provides an optional SATA Flash module with up to 16 GB NAND Flash memory. The SATA Flash module is connected to the CP3002 via the board-to-board connectors J5 located on the CP3002 and J1 located on the SATA Flash module. The SATA Flash module has been optimized for embedded systems providing high performance, reliability and security. The SATA Flash module cannot be used in conjunction with the CP3002-HDD module.

Note ...

Write protection is available for this module. Contact Kontron for further assistance if write protection is required.

Note ...

If the SATA Flash module is mounted on the CP3002, the CP3002-HDD module cannot be used on the CP3002.

Either the SATA Flash module or the CP3002-HDD module can be mounted on the CP3002.

C.1 Technical Specifications

Table C-1: SATA Flash Module Specifications

SATA FLASH MODULE		SPECIFICATIONS
Interface	Board-to-Board Connector	One 18-pin, female, board-to-board connector, J1
Memory	Memory	Up to 16 GB SLC-based NAND Flash memory • Built-in full hard disk emulation • Up to 50 MB/s read rate • Up to 45 MB/s write rate
General	Power Consumption	typ. 0.5 W 3.3 V supply
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +85°C Extended Storage: -40°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	38 mm x 27 mm
	Board Weight	ca. 7 grams

C.2 SATA Flash Module Layout

The SATA Flash module includes one board-to-board connector, J1, for connection to the CP3002.

Figure C-1: SATA Flash Module Layout (Top View)

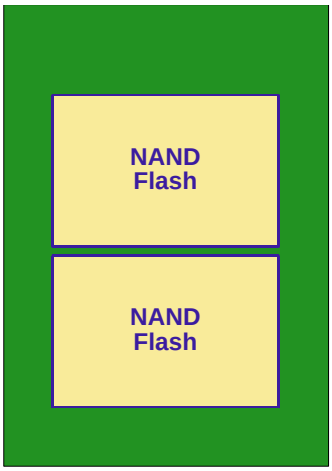

Figure C-2: SATA Flash Module Layout (Bottom View)