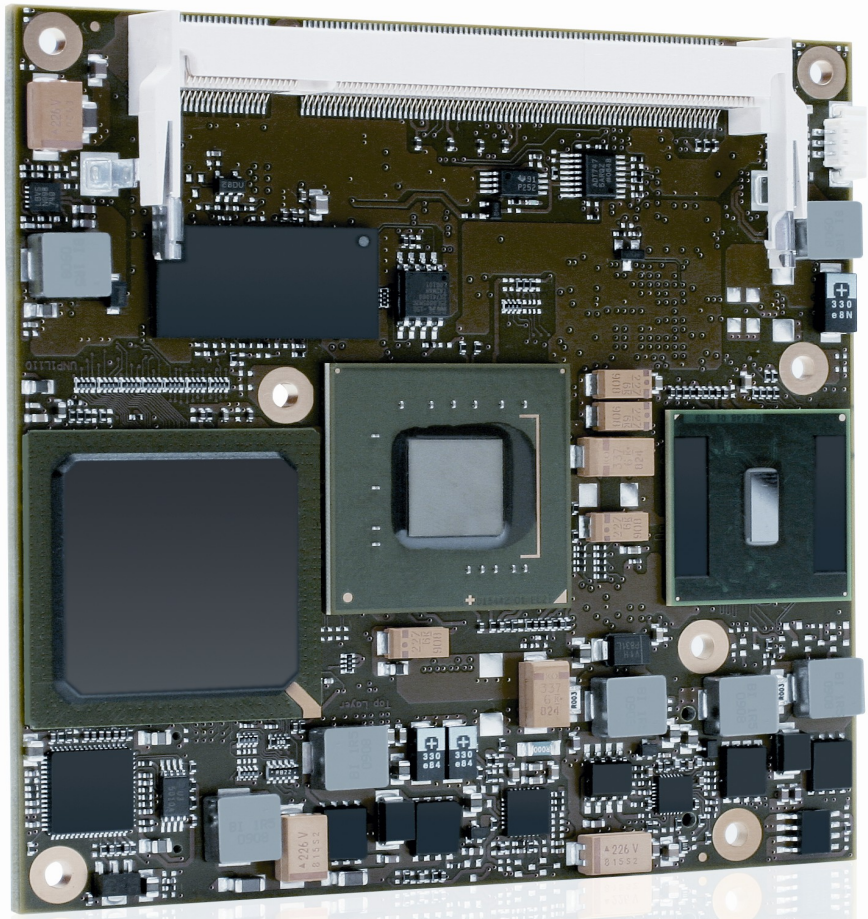
» Kontron User's Guide «



COMe-cDC2

Document Revision 130

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1 User Information

1.1 About This Document

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For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

1.2 Copyright Notice

1.3 Trademarks

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- » Microsoft is a registered trademark of Microsoft Corp.
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1.4 Standards

Kontron Europe GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Europe GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Europe GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Europe GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Europe GmbH that are caused by a faulty Kontron Europe GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Europe GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Please consult our Web site at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section http://emdcustomersection.kontron.com for the latest BIOS downloads, Product Change Notifications, Board Support Packages, DemoImages, 3D drawings and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 Product Description

The COMe-cDC2 brings latest 45 nm performance generations of Intel® Atom™ N270 processor with 1.6 GHz and the Intel® 945GSE and ICH7M chipset to a compact 95 x 95 mm module.

Kontron's new high-efficient power-off state S5 Eco enables ACPI features and lowest power-consumption in soft-off state – less than 1 mA. Compared to the regular S5 state this means a reduction by at least factor 200! Battery uptime therefore goes up dramatically.

Like all COM Express® compact modules, it is compatible to the COM Express® basic. Therefore, upgrading existing carrier boards originally designed for COM Express® basic gets easy and minimizes redesign efforts.

2.2 Naming clarification

COM Express® defines a Computer-On-Module, or COM, with all components necessary for a bootable host computer, packaged as a super component.

» COMe-bXX# modules are Kontron's COM Express® modules in basic form factor (125mm x 95mm), formerly known as ETXexpress®

» COMe-cXX# modules are Kontron's COM Express® modules in compact form factor (95mm x 95mm), formerly known as microETXexpress®

» COMe-mXX# modules are Kontron's COM Express® modules in mini form factor (55mm x 84mm), formerly known as nanoETXexpress

The product names for Kontron COM Express® Computer-on-Modules consist of a short form of the industry standard (**COMe-**), the form factor (**b**=basic, **c**=compact, **m**=mini), the capital letters for the CPU and Chipset Codenames (**XX**) and the pin-out type (**#**) followed by the CPU Name.

2.3 Understanding COM Express® Functionality

All Kontron COM Express® basic and compact modules contain two 220pin connectors; each of it has two rows called Row A & B on primary connector and Row C & D on secondary connector. COM Express® Computer-on-modules feature the following maximum amount of interfaces according to the PICMG module Pin-out type:

Feature	Pin-Out Type 1	Pin-Out Type 10	Pin-Out Type 2	Pin-Out Type 6
HD Audio	1x	1x	1x	1x
Gbit Ethernet	1x	1x	1x	1x
Serial ATA	4x	4x	4x	4x
Parallel ATA	-	-	1x	-
PCI	-	-	1x	-
PCI Express x1	6x	6x	6x	8x
PCI Express x16 (PEG)	-	-	1x	1x
USB Client	1x	1x	-	-
USB 2.0	8x	8x	8x	8x
USB 3.0	-	2x	-	4x
VGA	1x	-	1x	1x
LVDS	Dual Channel	Single Channel	Dual Channel	Dual Channel
DP++ (SDVO/DP/HDMI/DVI)	1x optional	1x	3x shared with PEG	3x
LPC	1x	1x	1x	1x
External SMB	1x	1x	1x	1x
External I2C	1x	1x	1x	1x
GPIO	8x	8x	8x	8x
SDIO	1x optional	1x optional	-	-
UART (2-wire COM)	-	2x	-	2x
FAN PWM out	-	1x	-	1x

2.4 COM Express® Documentation

This product manual serves as one of three principal references for a COM Express® design. It documents the specifications and features of COMe-cDC2. Additional references are are available from your Kontron Support or from PICMG®:

» The COM Express® Specification defines the COM Express® module form factor, pin-out, and signals. This document is available from the PIGMG website by filling out the order form.

» The COM Express® Design Guide by PICMG serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express® modules.

Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.5 COM Express® Benefits

COM Express® modules are very compact, highly integrated computers. All Kontron COM Express® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each COM is based on the COM Express® specification. This standardization allows designers to create a single-system baseboard that can accept present and future COM Express® modules.

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A single baseboard design can use a range of COM Express® modules with different size and pin-out. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of a COM Express® solution also ensures against obsolescence as computer technology evolves. A properly designed COM Express® baseboard can work with several successive generations of COM Express® modules.

A COM Express® baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Product Specification

3.1 Modules & Accessories

The COM Express® compact sized Computer-on-Module COMe-cDC2 (UNP1) follows pin-out Type 2 and is compatible to PICMG specification COM.0 Rev 1.0. The COMe-cDC2 based on Intel's Navy Pear platform is available in different variants:

Commercial grade modules (0°C to 60°C operating)

Product Number	Product Name	Processor	Chipset and Features
36005-0000-16-2	COMe-cDC2 N270	Intel® Atom™ N270	DDR2, 945GSE
36005-0040-16-2	COMe-cDC2 N270 4GB	Intel® Atom™ N270	DDR2, 945GSE, 4GB SSD

Extended temperature modules (E1, -25°C to +75°C operating)

Product Number	Product Name	Processor	Chipset and Features
36005-0000-16-2EXT	COMe-cDC2 N270 E1	Intel® Atom™ N270	DDR2, 945GSE, E1
36005-0040-16-2EXT	COMe-cDC2 N270 4GB E1	Intel® Atom™ N270	DDR2, 945GSE, 4GB SSD, E1

Accessories

Product Number	Carrier Boards
38102-0000-00-1	COM Express® Reference Carrier Type 2 (8mm COMe connector)
38104-0000-00-0	COM Express® Eval Carrier Type 2 (Niles Canyon, 5mm COMe connector)
38104-0000-00-1	COM Express® Eval Carrier Type 2 (Topanga Canyon, 5mm COMe connector)
Product Number	**Memory**
97011-5120-08-0	DDR2-800 SODIMM / 512MB
97011-1024-08-0	DDR2-800 SODIMM / 1GB
97011-2048-08-0	DDR2-800 SODIMM / 2GB
97011-5120-08-2	DDR2-800 SODIMM / 512MB E2
97011-1024-08-2	DDR2-800 SODIMM / 1GB E2
97011-2048-08-2	DDR2-800 SODIMM / 2GB E2
Product Number	**Cooling & Mounting**
36005-0000-99-0	HSP COMe-cDC2 thread
36005-0000-99-1	HSP COMe-cDC2 through
36005-0000-99-0C01	HSK COMe-cDC2 active thread
36005-0000-99-0C02	HSK COMe-cDC2 passive thread
36099-0000-99-0	COMe Active Uni Cooler (for CPUs up to 20W TDP)
36099-0000-99-1	COMe Passive Uni Cooler (for CPUs up to 10W TDP)
38017-0000-00-0	COMe Mount KIT 8mm 1set
38017-0000-00-5	COMe Mount KIT 5mm 1set
38017-0100-00-0	COMe Mount KIT 8mm 100sets
38017-0100-00-5	COMe Mount KIT 5mm 100sets
Product Number	**Adapter & Cables**
9-5000-0352	ADA-LVDS-DVI 18bit (LVDS to DVI converter)
96079-0000-00-0	KAB-HSP 200mm (Cable adapter to connect a standard FAN to the module)
96079-0000-00-1	KAB-HSP 40mm (Cable adapter to connect a standard FAN to the module)

3.2 Functional Specification

Processor

The 45nm Intel® ATOM™ (Diamondville) CPU with 22x22mm package size (PBGA437 socket) supports:

» Intel® Hyper-Threading Technology (HTT)

» Enhanced Intel SpeedStep® Technology (EIST)

» Thermal Monitoring Technologies

» Idle States (C-States)

» Execute Disable Bit

CPU specifications

» Intel® ATOM™

» Codename: Diamondville

» L2-Cache: 512kB

» FSB: 533MHz

» Instruction set: 32bit

Memory

Sockets	1x DDR2 SO-DIMM
Memory Type	DDR2-400/533
Maximum Size	2GB
Technology	Single Channel

Chipset

The Intel® 945GSE Chipset (Codename Calistoga) combined with the Intel® 82801GBM (ICH7M) Southbridge supports:

» PCI Express Revision 1.0

» USB 2.0

» Integrated Graphics with dual display

Graphics Core

The integrated Intel® GMA950 (Gen3.5) supports:

Graphics Core Render Clock	166MHz
Execution Units / Pixel Pipelines	4
Max Graphics Memory	256MB
GFX Memory Bandwidth (GB/s)	10.7
GFX Memory Technology	DVMT 3.0
API (DirectX/OpenGL)	9.0c / 1.4
Shader Model	2.0
Hardware accelerated Video	-
Independent/Simultaneous Displays	2
Display Port	-
HDCP support	-

Monitor output

CRT max Resolution	2048x1536
TV out:	YES

LVDS

LVDS Bits/Pixel	1x18 / 2x18
LVDS Bits/Pixel with dithering	-
LVDS max Resolution:	1600x1200
PWM Backlight Control:	YES
Supported Panel Data:	JILI2/JILI3/EDID/DID

Display Interfaces

Discrete Graphics	-
Digital Display Interface DDI1	SDVOB
Digital Display Interface DDI2	-
Digital Display Interface DDI3	-
Maximum Resolution on DDI	1920x1200

Storage

onboard SSD	512MB to 8GB SLC (PATA)
SD Card support	-
IDE Interface	1x PATA 100
Serial-ATA	2x SATA 1.5Gb/s
SATA AHCI	NCQ, HotPlug, Staggered Spinup
SATA RAID	-

Variants with onboard SSD flash do not support external IDE due to the missing signals PDIAG# and DASP# master/slave capabilities on COM Express® connector

Connectivity

USB	8x USB 2.0
USB Client	-
PCI	PCI Rev 2.3 (33MHz/3.3V)
PCI External Masters	4
PCI Express	3x PCIe x1 Gen1
Max PCI Express	4x PCIe x1 without LAN
PCI Express x2/x4 configuration	NO
Ethernet	10/100/1000 Mbit
Ethernet controller	Intel® 82574L (Hartwell)

Ethernet

The Intel® 82574L (Hartwell) ethernet supports:

» Jumbo Frames

» Time Sync Protocol Indicator

» WOL (Wake On LAN)

» PXE (Preboot eXecution Environment)

Misc Interfaces and Features

Audio	AC97 / HD Audio
Onboard Hardware Monitor	ON Semi ADT7475
Trusted Platform Module	Infineon TPM 1.2 SLB9635TT
Miscellaneous	-

Kontron Features

External I2C Bus	Fast I2C, MultiMaster capable
M.A.R.S. support	YES
Embedded API	JIDA16 / JIDA32 / PICMG EAPI
Custom BIOS Settings / Flash Backup	YES
Watchdog support	Dual Staged

Power Features

Singly Supply Support	YES
Supply Voltage	8.5V - 18V
ACPI	ACPI 2.0
S-States	S0, S3, S4, S5
S5 Eco Mode	YES
Misc Power Management	DPST 2.3

Power Consumption and Performance

Full Load Power Consumption	10W
Kontron Performance Index	1714
Kontron Performance/Watt	172

Detailed Power Consumption measurements in all states and bechmarks for CPU, Graphics and Memory performance are available in Application Note KEMAP054 at EMD Customer Section.

Supported Operating Systems

The COMe-cDC2 currently supports:

» Microsoft Windows CE 6.0

» Microsoft Windows XP embedded

» Microsoft Windows XP x86

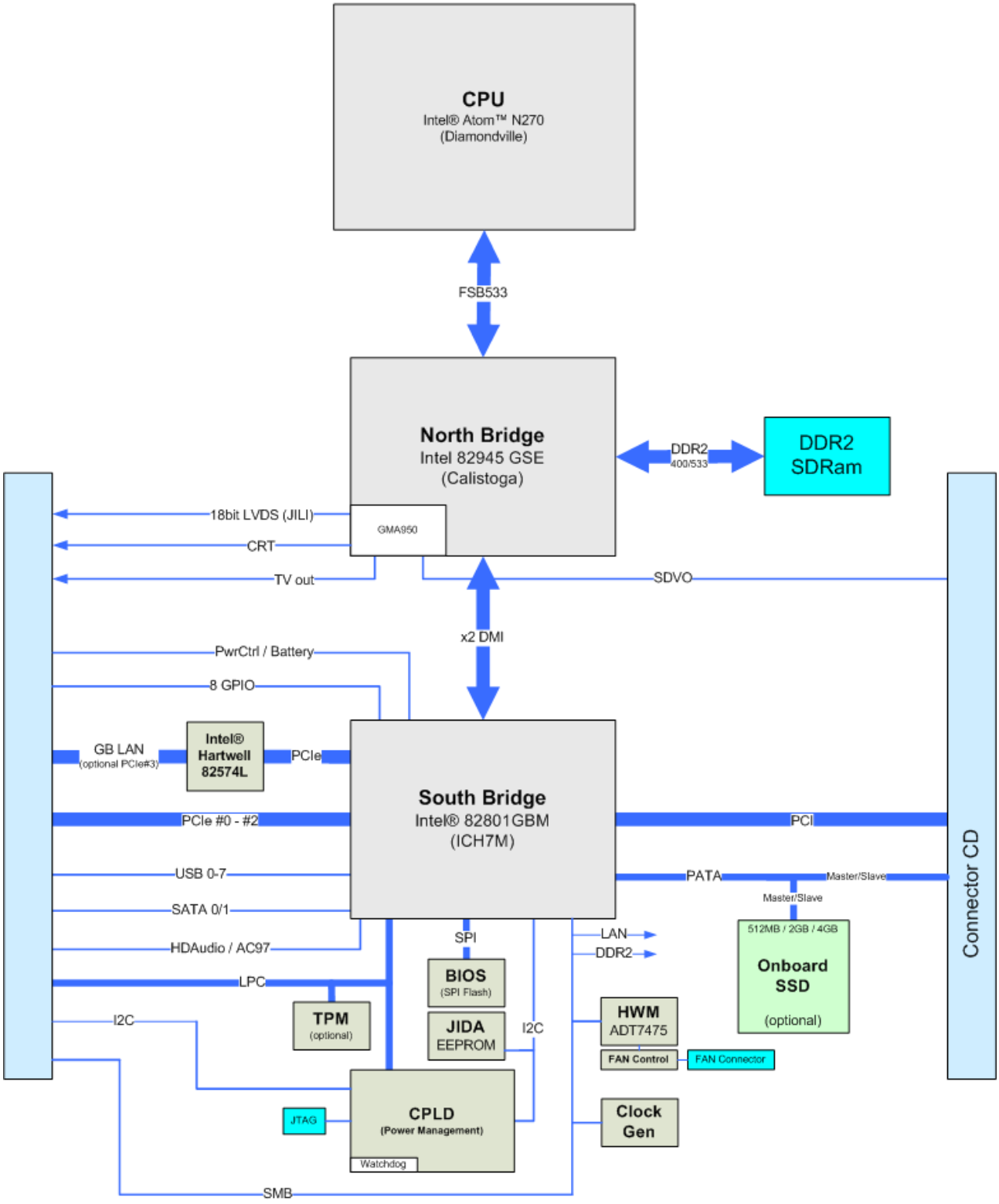
» Microsoft Windows 7 x86

» Microsoft Windows Embedded Standard 7 x86 (WES7)

» Linux

» WindRiver VxWorks 6.6 - 6.8

3.3 Block Diagram



3.4 Electrical Specification

3.4.1 Supply Voltage

Following supply voltage is specified at the COM Express® connector:

VCC:	8.5V - 18V
Standby:	5V DC +/- 5%
RTC:	2.5V - 3.3V

- 5V Standby voltage is not mandatory for operation.
- Extended Temperature (E1) variants are validated for 12V supply only

3.4.2 Power Supply Rise Time

» The input voltages shall rise from ≤10% of nominal to within the regulation ranges within 0.1ms to 20ms.

» There must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of its final set-point following the ATX specification

3.4.3 Supply Voltage Ripple

» Maximum 100 mV peak to peak 0 – 20 MHz

3.4.4 Power Consumption

The maximum Power Consumption of the different COMe-cDC2 variants is 10W (100% CPU load on all cores; 90°C CPU temperature). Further information with detailed measurements are available in Application Note KEMAP054 available on EMD Customer Section. Information there is available after registration.

3.4.5 ATX Mode

By connecting an ATX power supply with VCC and 5VSB, PWR_OK is set to low level and VCC is off. Press the Power Button to enable the ATX PSU setting PWR_OK to high level and powering on VCC. The ATX PSU is controlled by the PS_ON# signal which is generated by SUS_S3# via inversion. VCC can be 8.5V - 18V in ATX Mode. On Computer-on-Modules supporting a wide range input down to 4.75V the input voltage shall always be higher than 5V Standby (VCC > 5VSB).

State	PWRBTN#	PWR_OK	V5_StdBy	PS_ON#	VCC
G3	x	x	0V	x	0V
S5	high	low	5V	high	0V
S5 → S0	PWRBTN Event	low → high	5V	high → low	0 V→ VCC
S0	high	high	5V	low	VCC

3.4.6 Single Supply Mode

In single supply mode (or automatic power on after power loss) without 5V Standby the module will start automatically when VCC power is connected and Power Good input is open or at high level (internal PU to 3.3V). PS_ON# is not used in this mode and VCC can be 8.5V - 18V.

To power on the module from S5 state press the power button or reconnect VCC. Suspend/Standby States are not supported in Single Supply Mode.

State	PWRBTN#	PWR_OK	V5_StdBy	VCC
G3	x	x	x	0
G3 → S0	high	open / high	x	connecting VCC
S5	high	open / high	x	VCC
S5 → S0	PWRBTN Event	open / high	x	reconnecting VCC

Signals marked with “x” are not important for the specific power state. There is no difference if connected or open.

All ground pins have to be tied to the ground plane of the carrier board.

3.5 Power Control

Power Supply

The COMe-cDC2 supports a power input from 8.5V - 18V. The supply voltage is applied through the VCC pins (VCC) of the module connector.

Power Button (PWRBTN#)

The power button (Pin B12) is available through the module connector described in the pinout list. To start the module via Power Button the PWRBTN# signal must be at least 50ms (50ms ≤ t < 4s, typical 400ms) at low level (Power Button Event).

Pressing the power button for at least 4seconds will turn off power to the module (Power Button Override).

Power Good (PWR_OK)

The COMe-cDC2 provides an external input for a power-good signal (Pin B24). The implementation of this subsystem complies with the COM Express® Specification. PWR_OK is internally pulled up to 3.3V and must be high level to power on the module.

Reset Button (SYS_RESET#)

The reset button (Pin B49) is available through the module connector described in the pinout list. The module will stay in reset as long as SYS_RESET# is grounded. If available, the BIOS setting for “Reset Behavior” must be set to “Power Cycle”.

Modules with Intel® Chipset and active Management Engine does not allow to hold the module in Reset out of S0 for a long time. At about 10s holding the reset button the ME will reboot the module automatically

SM-Bus Alert (SMB_ALERT#)

With an external battery manager present and SMB_ALERT# (Pin B15) connected the module always powers on even if BIOS switch “After Power Fail” is set to “Stay Off”.

3.6 Environmental Specification

3.6.1 Temperature Specification

General Specification	Operating	Non-operating
Commercial grade	0°C to +60°C	-30°C to +85°C
Extended (E1)	-25°C to +75°C	-30°C to +85°C
Industrial grade (E2)	-40°C to +85°C	-40°C to +85°C

Standard modules are available for commercial grade temperature range. Please see chapter Product Specification for available variants for extended or industrial temperate grade

With Kontron heatspreader plate assembly

The operating temperature defines two requirements:

» the maximum ambient temperature with ambient being the air surrounding the module.

» the maximum measurable temperature on any spot on the heatspreader's surface

Without Kontron heatspreader plate assembly

The operating temperature is the maximum measurable temperature on any spot on the module's surface.

3.6.2 Humidity

» Operating: 10% to 90% (non condensing)

» Non operating: 5% to 95% (non condensing)

3.7 Standards and Certifications

RoHS

The **COMe-cDC2** is compliant to the directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.

CE marking

The **COMe-cDC2** is CE marked according to Low Voltage Directive 2006/95/EC – Test standard EN60950

Component Recognition UL 60950-1

The **COM Express® compact** form factor Computer-on-Modules are Recognized by Underwriters Laboratories Inc. Representative samples of this component have been evaluated by UL and meet applicable UL requirements.

UL Listings:

» NWGQ2.E304278

» NWGQ8.E304278

WEEE Directive

WEEE Directive 2002/96/EC is not applicable for Computer-on-Modules.

Conformal Coating

Conformal Coating is available for Kontron Computer-on-Modules and for validated SO-DIMM memory modules. Please contact your local sales or support for further details.

Shock & Vibration

The **COM Express® compact** form factor Computer-on-Modules successfully passed shock and vibration tests according to

» IEC/EN 60068-2-6 (Non operating Vibration, sinusoidal, 10Hz-4000Hz, +/-0.15mm, 2g)

» IEC/EN 60068-2-27 (Non operating Shock Test, half-sinusoidal, 11ms, 15g)

EMC

Validated in Kontron reference housing for EMC the **COMe-cDC2** follows the requirements for electromagnetic compatibility standards

» EN55022

» EN55011

» EN55024

» FCC15

3.8 MTBF

The following MTBF (Mean Time Before Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.

The calculation methode used is "Telcordia Method 1 Case 3" in a ground benign, controlled environment (GB,GC). This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned in.

Other environmental stresses (extreme altitude, vibration, salt water exposure, etc) lower MTBF values.

System MTBF (hours): 199784 @ 40°C

Fans usually shipped with Kontron Europe GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

3.9 Mechanical Specification

Dimension

» 95.0 mm x 95.0 mm (3.75” x 3.75”)

» Hight approx. 12mm (0.4”)

CAD drawings are available at EMD CustomerSection

3.10 Thermal Management

A heatspreader plate assembly is available from Kontron Europe GmbH for the COMe-cDC2. The heatspreader plate on top of this assembly is NOT a heat sink. It works as a COM Express®-standard thermal interface to use with a heat sink or other cooling device.

External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heatspreader assembly implement thermal interfaces between the heatspreader plate and the major heat-generating components on the COMe-cDC2. About 80 percent of the power dissipated within the module is conducted to the heatspreader plate and can be removed by the cooling solution.

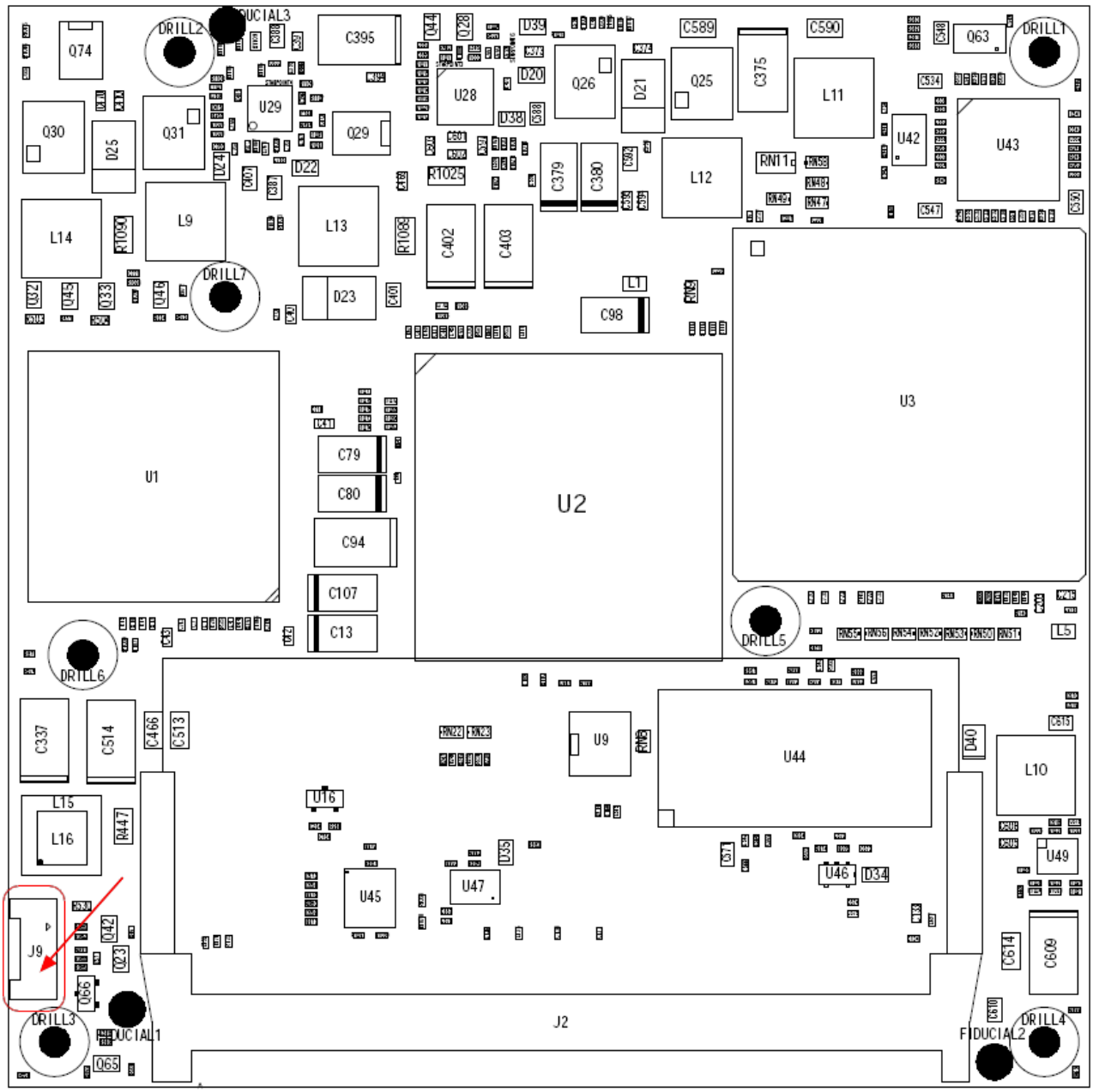
You can use many thermal-management solutions with the heatspreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COM Express® application and environmental conditions. Please see the COM Express® Design Guide for further information on thermal management.

3.11 Heatspreader

Documentation and CAD drawings of COMe-cDC2 heatspreader and cooling solutions is provided at http://emdcustomersection.kontron.com.

3.12 Onboard Fan Connector

Location and Pinout of Fan Connector



The onboard fan connector (J9) can be found at the left side nearby the DRAM socket and has following specification:

» Part number (Molex) J9: 53261-0390

» Mates with: 51021-0300

» Crimp terminals: 50079-8100

The Pin assignement is:

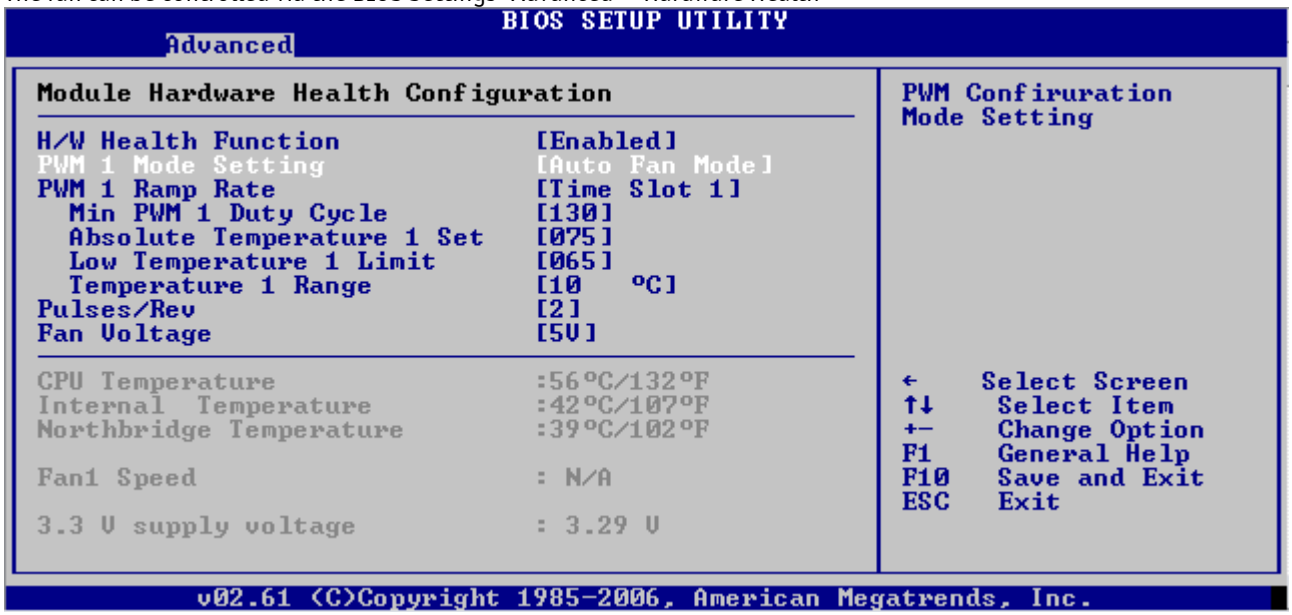
» Pin1: Tacho

» Pin2: VCC

» Pin3: GND

BIOS Settings for Fan Control

The fan can be controlled via the BIOS Settings “Advanced → Hardware Health”



In general 4 modes are possible

» Auto Fan Mode: Temperature Values can be selected to control the Fan

» Fan Always On Full: Fan is always full on

» Fan Disable Mode: Fan is disabled

» Fan Manually Mode: A fixed PWM value (0...255) can be entered to run the fan at a selected speed

The used hardware monitor onboard is an ADT7475. For additional information please refer to the regarding datasheet.

3.12.1 Electrical Characteristics

Input Voltage Range	8.5V - 18V
Output Voltage	Only 12V (switch in BIOS without function)
Max. output current	0.3A

The Fan out voltage output is not short circuit proof. If necessary the user has to ensure that the circuit is protected externally, for example by a fuse on the backplane.

To connect a standard FAN with 3pin connector to the module please use adaptor cable KAB-HSP 200mm (96079-0000-00-0) or KAB-HSP 40mm (96079-0000-00-2)

4 Features and Interfaces

4.1 Onboard SSD

The COMe-cDC2 features an onboard Greenliant PATA NAND flash drive with capacities of 512MB to 8GB SLC (PATA). Due to performance and longevity reasons standard variants with onboard flash use SLC type only. The following PATA NANDrives are available:

Basic features of the PATA NANDrives

» 16-bit ATA/IDE Bus Interface with PIO Mode-6, Multi-Word DMA Mode-4 and Ultra DMA Mode-4

» RoHS compliant NAND flash type

» Hardware error detection and correction ECC

» Advanced wear leveling

» Bad block management

SLC NANDrive™

Flash Part No.	GLS85LP0512P-S-I-LBTE	GLS85LP1002P-S-I-FTE	GLS85LP1004P-S-I-FTE	GLS85LP1008P-S-I-FTE
Temperature Range	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
Flash Size	**512MB**	**2GB**	**4GB**	**8GB**
NAND Type	SLC NAND	SLC NAND	SLC NAND	SLC NAND
Sustained Read Speed	25 MB/s	28 MB/s	50 MB/s	50 MB/s
Sustained Write Speed	6 MB/s	11 MB/s	20 MB/s	39 MB/s
Total Bytes	456,744,960	2,000,388,096	4,068,384,768	8,136,769,536
Max LBA	892,080	3,907,008	7,946,064	15,892,128
Cylinders/Heads/Sectors	885/16/63	3,876/16/63	7,883/16/63	15,766/16/63
Active Mode Power	200mW	200mW	265mW	365mW
Program/Erase Cycles per Block	100k	100k	100k	100k

(Data based on GLS85LPxxxxP Datasheet Rev. 02.000 from 06-2012)

The NAND Flash types listed above are available on COMe-mSP1 hardware revision CE4.7.0 and COMe-cDC2 hardware revision CE 2.4.1 or newer. Please contact your local sales or support for Flash specifications of SST Flash used on older revisions

4.2 S5 Eco Mode

Kontron's new high-efficient power-off state S5 Eco enables lowest power-consumption in soft-off state – less than 1 mA compared to the regular S5 state this means a reduction by at least factor 200!

In the "normal" S5 mode the board is supplied by 5V_Stb and needs usually up to 300mA just to stay off. This mode allows to be switched on by power button, RTC event and WakeOnLan, even when it is not necessary. The new S5 Eco mode reduces the current tremendously.

The S5 Eco Mode can be enabled in BIOS Setup, when the BIOS supports this feature.

Following prerequesites and consequences occur when S5 Eco Mode is enabled

» The power button must be pressed at least for 200ms to switch on.

» Wake via Powerbutton only.

» "Power On After Power Fail"/"State after G3": only "stay off" is possible

4.3 LPC

The Low Pin Count (LPC) Interface signals are connected to the LPC Bus bridge located in the CPU or chipset. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combines legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide maintained by PICMG. Please refer to the official PICMG documentation for additional information.

The LPC bus does not support DMA (Direct Memory Access) and a clock buffer is required when more than one device is used on LPC. This leads to limitations for ISA bus and SIO (standard I/O´s like Floppy or LPT interfaces) implementations.

All Kontron COM Express® Computer-on-Modules imply BIOS support for following external baseboard LPC Super I/O controller features for the **Winbond/Nuvoton 5V 83627HF/G and 3.3V 83627DHG-P**:

83627HF/G	Phoenix BIOS	AMI CORE8	AMI Aptio
PS/2	YES	YES	YES
COM1/COM2	YES	YES	YES
LPT	YES	YES	YES
HWM	YES	YES	NO
Floppy	NO	NO	NO
GPIO	NO	NO	NO
83627DHG-P	**Phoenix BIOS**	**AMI CORE8**	**AMI Aptio**
PS/2	YES	YES	YES
COM1/COM2	YES	YES	YES
LPT	YES	YES	YES
HWM	NO	NO	NO
Floppy	NO	NO	NO
GPIO	NO	NO	NO

Features marked as not supported do not exclude OS support (e.g. HWM can be accessed via SMB). For any other LPC Super I/O additional BIOS implementations are necessary. Please contact your local sales or support for further details.

4.4 LPC boot

The COMe-cDC2 supports boot from an external Firmwarehub on LPC bus (LPC FWH). The external LPC FWH can be activated with signal A34 “BIOS_DISABLE#” or according newer specifications “BIOS_DIS0#” in following configuration:

BIOS_DIS0#	BIOS_DIS1#	Function
open	open	Boot on-module BIOS
GND	open	Boot baseboard LPC FWH
open	GND	Baseboard SPI = Boot Device 1, on-module SPI = Boot Device 2
GND	GND	Baseboard SPI = Boot Device 2, on-module SPI = Boot Device 1

Using an external LPC Firmware Hub

To program an external LPC FWH follow these steps:

» Connect a 1MB LPC FWH to the module's LPC interface

» Open pin A34 to boot from the module BIOS

» Boot the module to DOS with access to the BIOS image and Firmware Update Utility aufdos.exe / batch file provided on EMD Customer Section

» Connect pin A43 (BIOS_DIS0#) to ground to enable the external LPC FWH

» Execute Flash.bat to flash the BIOS image to the external LPC FWH

» reboot

Your module will now boot from the external LPC FWH when BIOS_DIS0# is grounded.

To create a BIOS with custom defaults:

» Change your BIOS settings

» Save as custom defaults to RTC/Flash and Exit (module will now always start with these settings)

» Extract the BIOS including custom defaults with **afudos.exe biosname.rom /O** in DOS or **kflash.exe backup biosname.rom** in Windows

Flash Backup should show “Enter new Password” first time saving custom defaults. If it is not possible to set a new password or entering a password shows an error message, please clean up CMOS data with DOS command: **jidacmos rtc /clean** (jidacmos utility is available at Kontron’s Customer Section)

You can download all AMI CORE8 update utilities at AMI.com:
http://www.ami.com/support/downloads/amiflash.zip

4.5 M.A.R.S.

The Smart Battery implementation for Kontron Computer-on-Modules called **M**obile **A**pplication for **R**echargeable **S**ystems is a BIOS extension for external Smart Battery Manager or Charger. It includes support for SMBus charger/selector (e.g. Linear Technology LTC1760 Dual Smart Battery System Manager) and provides ACPI compatibility to report battery information to the Operating System.

Reserved SM-Bus addresses for Smart Battery Solutions on the carrier:

8-bit Address	7-bit Address	Device
12h	0x09	SMART_CHARGER
14h	0x0A	SMART_SELECTOR
16h	0x0B	SMART_BATTERY

4.6 Fast I2C

The COMe-cDC2 supports a CPLD implemented LPC to I2C bridge using the WISHBONE I2C Master Core provided from opencores.org. The I2C Interface supports transfer rates up to 40kB/s and can be configured in Setup

Specification for external I2C:

» Speed up to 400kHz

» Compatible to Philips I2C bus standard

» Multi-Master capable

» Clock stretching support and wait state generation

» Interrupt or bit-polling driven byte-by-byte data-transfers

» Arbitration lost interrupt with automatic transfer cancellation

» Start/Stop signal generation/detection

» Bus busy detection

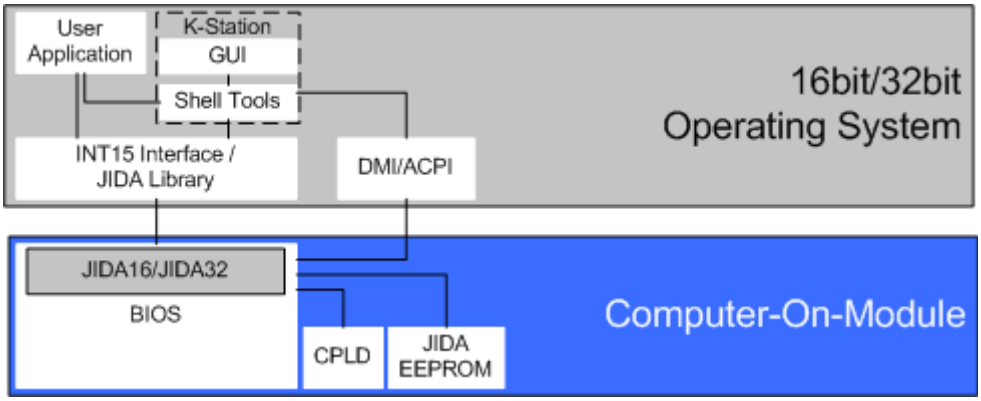
» 7bit and 10bit addressing

4.7 JIDA16 and JIDA32

JIDA16 (JUMPtec® Intelligent Device Architecture) is a BIOS interface which allows programs running in Real Mode operating systems (i.e. MS DOS) to call certain functions implemented in the BIOS. These functions can be used to get module information, make settings and access the I2C Bus and the Watchdog unit. JIDA16 functions are INT 15h BIOS calls which are only available in 16 Bit Real Mode operating systems.

For 32bit operating systems (i.e. WindowsXP, Windows 7, Windows CE, VxWorks, Linux) a different JIDA implementation called JIDA32 is implemented. The same common driver for all JIDA32 capable modules talks to the JIDA32 part in the BIOS, which is hardware dependent to interact with the hardware.

Please refer to EMD Customer Section for detailed documentation, JIDA utilities and Libraries for DOS, Windows, Linux, VxWorks or QNX.



Usage of JIDA16 and JIDA32

4.8 K-Station 1

Based on the JIDA32 interface users can implement advanced board functionality in their application. As an example utility Kontron provides K-Station for most 32bit Windows Operating Systems. K-Station 1 is a summary of command line utilities (Shell Tools) for easy access to JIDA32 BIOS implementations. Second part of K-Station is a JAVA based example GUI which gives a view an all available features using the Shell Tools.

Following K-Station Shell Tools are available:

- KSystemSummary.exe (System Information)
- KGenInfo.exe (Module Information)
- KCPUPerf.exe (CPU Throttling control)
- KHWMon.exe (Hardware Monitoring)
- KI2CBus.exe (I2C and SMBus access)
- KIOPort.exe (GPIO control)
- KStorage.exe (JIDA EEPROM access to user bytes)
- KVGATool.exe (LVDS Backlight control)
- KWDog.exe (Watchdog control)
- KAMIMod.exe (AMICore8 BIOS Modification with Bootlogo or Usercode ...)
- KFlash.exe (AMICore8 BIOS Update)

The full K-Station package, the stand-alone Shell Tools with drivers, example batch files and documentation is available on EMD Customer Section for free.

4.9 K-Station & API Resources for JIDA32

Available resources for default JIDA32 BIOS implementation and API:

4.9.1 I2C

BUS	Function
I2C 0	Internal / JIDA I2C
I2C 1	SM-Bus
I2C 2	external I2C
I2C 3	JILI DDC

4.9.2 Storage

Device	Function
EEPROM 0	JIDA EEPROM Area1 with 32 Bytes (free to use)

4.9.3 GPIO

Port	Function
IO-Port 0	GPI 0
IO-Port 1	GPI 1
IO-Port 2	GPI 2
IO-Port 3	GPI 3
IO-Port 4	GPO 0
IO-Port 5	GPO 1
IO-Port 6	GPO 2
IO-Port 7	GPO 3

4.9.4 Hardware Monitor

Sensor	Function
Temp 0	CPU temperature
Temp 1	internal HWM temperature (inside ADT7475)
Temp 2	chipset temperature (Northbridge
Temp 3	external carrier board SIO Winbond 83627 Temp Sensor 0
Temp 3	external carrier board SIO Winbond 83627 Temp Sensor 1
Temp 5	external carrier board SIO Winbond 83627 Temp Sensor 2
Temp 6	CPU Temperature (DTS)
Voltage 0	ADT7475 VCC : 3.3V S0
Voltage 1	external SIO Winbond 83627 CPU core voltage sensor: V CoreA
Voltage 2	external SIO Winbond 83627 CPU core voltage sensor: V CoreB
Voltage 3	external SIO Winbond 83627 battery voltage Sensor: VBAT
Voltage 4	external SIO Winbond 83627 Voltage Sensor 3: +3.3V
Voltage 5	external SIO Winbond 83627 Voltage Sensor 4: +5V
Voltage 6	external SIO Winbond 83627 standby Voltage Sensor 5: +5V sb
Voltage 6	external SIO Winbond 83627 Voltage Sensor: +12V

4.10 API Ressources for Board Driver

Available API ressources if Kontron Board Driver for JIDA32 & EAPI is used:

4.10.1 I2C

BUS	Type	Constant
I2C 0	External	JIDA_I2C_TYPE_EXT_I2C
I2C 1	SMBus	JIDA_I2C_TYPE_SMB
I2C 2	CRT	JIDA_I2C_TYPE_CRT
I2C 3	LVDS/JILI	JIDA_I2C_TYPE_JILI
I2C 4	SDVO	JIDA_I2C_TYPE_VIDEO
I2C 5	SDVO Channel B DDC1	JIDA_I2C_TYPE_SDVOB_DDC1
I2C 6	SDVO Channel B DDC2	JIDA_I2C_TYPE_SDVOB_DDC2
I2C 7	SDVO Channel C DDC1	JIDA_I2C_TYPE_SDVOC_DDC1
I2C 8	SDVO Channel C DDC2	JIDA_I2C_TYPE_SDVOC_DDC2
I2C 9	Internal	JIDA_I2C_TYPE_PRIMARY

4.10.2 Storage

Device	Function
EEPROM 0	JIDA EEPROM Area1 with 32 Bytes (free to use)

4.10.3 GPIO

Port	Function
IO-Port 0	GPI0 Port Bit 0-3: Input Bit 4-7: Output

4.10.4 Onboard Hardware Monitor

Sensor	Function
Temp 0	CPU Temperature (measured with ADT7475 HWM)
Temp 1	Board Temperature (internal IC temperature of onboard ADT7475 HWM)
Temp 2	Chipset Temperature
FAN 0	Onboard CPU FAN
Voltage 0	Module RTC Battery input
Voltage 1	Module 3.3V S0 voltage

4.10.5 SIO Winbond 83627DHGP

Sensor is only available if external carrier board SIO Windbond/Nuvoton 83627DHGP is present

Sensor	Function
Temp 3	Temp Sensor 1 (SYSTIN)
Temp 4	Temp Sensor 2 (CPUTIN)
Temp 5	Temp Sensor 3 (AUXTIN)
FAN 1	FAN Sensor 0 (SYSFANIN)
FAN 2	FAN Sensor 1 (CPUFANIN0)
FAN 3	FAN Sensor 2 (AUXFANIN0)
FAN 4	FAN Sensor 3 (SYSFANIN1)
Voltage 2	Voltage Sensor 0: VCore
Voltage 3	Voltage Sensor 1: VIN0
Voltage 4	Voltage Sensor 2: AVCC
Voltage 5	Voltage Sensor 3: 3VCC
Voltage 6	Voltage Sensor 4: VIN1
Voltage 7	Voltage Sensor 5: VIN2
Voltage 8	Voltage Sensor 6: VIN3
Voltage 9	Voltage Sensor 7: 3VSB
Voltage 10	Voltage Sensor 8: VBAT

4.10.6 SIO Winbond 83627HG

Sensor is only available if external carrier board SIO Windbond/Nuvoton 83627HG is present

Sensor	Function
Temp 3	Temp Sensor 1 (SYSTIN)
Temp 4	Temp Sensor 2 (CPUTIN)
Temp 5	Temp Sensor 3 (AUXTIN)
FAN 1	FAN Sensor 0 (SYSFANIN)
FAN 2	FAN Sensor 1 (CPUFANIN0)
FAN 3	FAN Sensor 2 (AUXFANIN0)
FAN 4	FAN Sensor 3 (SYSFANIN1)
Voltage 2	Voltage Sensor 0: VCoreA
Voltage 3	Voltage Sensor 1: VCoreB
Voltage 4	Voltage Sensor 2: +3.3V VIN
Voltage 5	Voltage Sensor 3: +5V AVCC
Voltage 6	Voltage Sensor 4: +12V VIN
Voltage 7	Voltage Sensor 5: -12V VIN
Voltage 8	Voltage Sensor 6: -5V VIN
Voltage 9	Voltage Sensor 7: VSB
Voltage 10	Voltage Sensor 8: VBAT

The shown resource assignment is valid for Windows operating systems with standard API and hardware configuration only. There may be OS specific and customized assignments that differ from the tables shown in this chapter. Please have a look at the API documentation for additional information.

4.11 GPIO - General Purpose Input and Output

The COMe-cDC2 offers 4 General Purpose Input (GPI) pins and 4 General Purpose Output (GPO) pins. On a 3.3V level digital in- and outputs are available.

Signal	Pin	Description
GPI0	A54	General Purpose Input 0
GPI1	A63	General Purpose Input 1
GPI2	A67	General Purpose Input 2
GPI3	A85	General Purpose Input 3
GPO0	A93	General Purpose Output 0
GPO1	B54	General Purpose Output 1
GPO2	B57	General Purpose Output 2
GPO3	B63	General Purpose Output 3

Configuration

The GPI and GPO pins can be configured via JIDA32/K-Station. Please refer to the JIDA32/K-Station manual in the driver download packet on our customer section.

4.12 Dual Staged Watchdog Timer

Basics

A watchdog timer (or computer operating properly (COP) timer) is a computer hardware or software timer that triggers a system reset or other corrective action if the main program, due to some fault condition, such as a hang, neglects to regularly service the watchdog (writing a “service pulse” to it, also referred to as “kicking the dog”, “petting the dog”, “feeding the watchdog” or “triggering the watchdog”). The intention is to bring the system back from the nonresponsive state into normal operation.

The COMe-cDC2 offers a watchdog which works with two stages that can be programmed independently and used one by one.

Time-out events

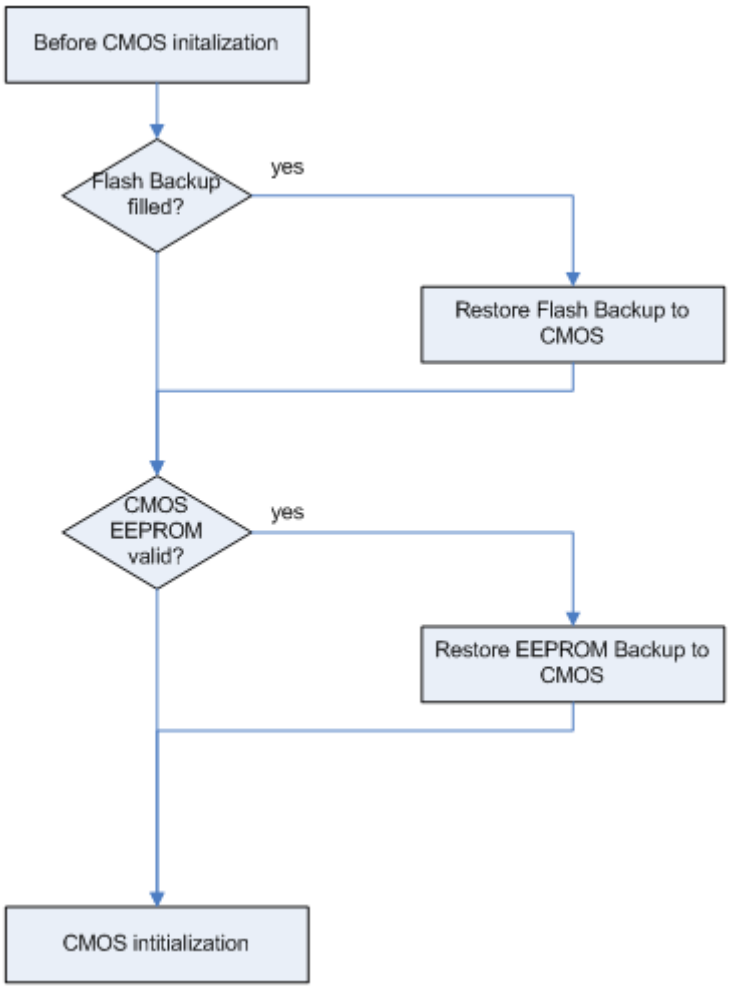
Reset	A reset will restart the module and starts POST and operating system new.
NMI	A non-maskable interrupt (NMI) is a computer processor interrupt that cannot be ignored by standard interrupt masking techniques in the system. It is typically used to signal attention for non-recoverable hardware errors.
SCI	A system control interrupt (SCI) is a OS-visible interrupt to be handled by the OS using AML code
Delay	Might be necessary when an operating system must be started and the time for the first trigger pulse must extended. (Only available in the first stage)
WDT Signal only	This setting triggers the WDT Pin on baseboard connector (COM Express® Pin B27) only
Cascade:	Does nothing, but enables the 2nd stage after the entered time-out.

WDT Signal

B27 on COM Express® Connector offers a signal that can be asserted when a watchdog timer has not been triggered within time. It can be configured to any of the 2 stages. Deassertion of the signal is automatically done after reset. If deassertion during runtime is necessary please ask your Kontron technical support for further help.

4.13 Flash Backup Feature

The COMe-cDC2 supports a new functionality called “Flash Backup”. This new feature allows saving custom defaults directly into the Flash. With invalid EEPROM data or without a CMOS EEPROM, the module will start up with these custom defaults. It’s possible to save this BIOS with changed defaults to an image and flash it on other modules.



To create a BIOS with custom defaults:

» Change your BIOS settings

» Save as custom defaults to RTC/Flash and Exit (module will now always start with these settings)

Flash Backup should show “Enter new Password” first time saving custom defaults. If it is not possible to set a new password or entering a password shows an error message, please clean up CMOS data with DOS command: **jidacmos rtc /clean** (jidacmos utility is available at Kontron’s Customer Section)

» Extract the BIOS including custom defaults with afudos or kflash utility for windows

Tool	Command
AFUDOS	`c:\>afudos.exe biosname.rom /O`
KFLASH	`c:\>kflash.exe backup biosname.rom`

Flash your BIOS with custom defaults:

To flash a BIOS with customized defaults extracted like described above, use following options

Operating System	Command
Windows OS	`c:\>kflash.exe flash biosname.rom /bncr`
DOS	`c:\>afudos.exe biosname.rom /p /b /n /c` `c:\>jidacmos.exe eep /clean`

kflash.exe is a shell tool included in Kontron K-Station System Utility Package.
jidacmos utility is included in the BIOS download packages at Kontron's customer section.

4.14 Speedstep Technology

The Intel® processors offers the Intel® Enhanced SpeedStep™ technology that automatically switches between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. It let you customize high performance computing on your applications. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage, conserving battery life while maintaining a high level of performance. The frequency is set back automatically to the high frequency, allowing you to customize performance.

In order to use the Intel® Enhanced SpeedStep™ technology the operating system must support SpeedStep™ technology.

By disabling the SpeedStep feature in the BIOS, manual control/modification of CPU performance is possible. Setup the CPU Performance State in the BIOS Setup or use 3rd party software to control CPU Performance States.

4.15 C-States

New generation platforms include power saving features like SuperLFM, EIST (P-States) or C-States in O/S idle mode.

Activated C-States are able to dramatically decrease power consumption in idle mode by reducing the Core Voltage or switching of parts of the CPU Core, the Core Clocks or the CPU Cache.

Following C-States are defined:

C-State	Description	Function
C0	Operating	CPU fully turned on
C1	Halt State	Stops CPU main internal clocks via software
C1E	Enhanced Halt	Similar to C1, additionally reduces CPU voltage
C2	Stop Grant	Stops CPU internal and external clocks via hardware
C2E	Extended Stop Grant	Similar to C2, additionally reduces CPU voltage
C3	Deep Sleep	Stops all CPU internal and external clocks
C3E	Extended Stop Grant	Similar to C3, additionally reduces CPU voltage
C4	Deeper Sleep	Reduces CPU voltage
C4E	Enhanced Deeper Sleep	Reduces CPU voltage even more and turns off the memory cache
C6	Deep Power Down	Reduces the CPU internal voltage to any value, including 0V
C7	Deep Power Down	Similar to C6, additionally LLC (LastLevelCache) is switched off

C-States are usually enabled by default for low power consumption, but active C-States my influence performance sensitive applications or real-time systems.

» Active C6-State may influence data transfer on external Serial Ports

» Active C7-State may cause lower CPU and Graphics performance

It's recommended to disable C-States / Enhanced C-States in BIOS Setup if any problems occur.

4.16 Hyper Threading

Hyper Threading (officially termed Hyper Threading Technology or HTT) is an Intel®-proprietary technology used to improve parallelization of computations performed on PC´s. Hyper-Threading works by duplicating certain sections of the processor—those that store the architectural state but not duplicating the main execution resources. This allows a Hyper-Threading equipped processor to pretend to be two “logical” processors to the host operating system, allowing the operating system to schedule two threads or processes simultaneously. Hyper Threading Technology support always relies on the Operating System.

4.17 ACPI Suspend Modes and Resume Events

The COMe-cDC2 supports the S3 state (=Save to Ram). S4 (=Save to Disk) is not supported by the BIOS (S4_BIOS) but S4_OS is supported by the following operating systems:

» Windows XP

» Windows Vista

» Windows 7

The following events resume the system from S3:

» USB Keyboard (1)

» USB Mouse (1)

» Power Button

» WakeOnLan (2)

The following events resume the system from S4:

» Power Button

» WakeOnLan (2)

The following events resume the system from S5:

» Power Button

» WakeOnLan (2)

(1) OS must support wake up via USB devices and baseboard must power the USB Port with StBy-Voltage

(2) WakeOnLan must be enabled in BIOS setup and driver options

5 System Ressources

5.1 Interrupt Request (IRQ) Lines

Please be aware that an ACPI OS decides itself on resource usage. The tables below show only an example distribution.

5.1.1 In 8259 PIC Mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	-
1	Keyboard	No	-
2	Slave 8259	No	-
3	COM2	Yes	Note(1)
4	COM1	Yes	Note(1)
5	Free	Yes	-
6	Floppy Drive Controller	Yes	Note(1)
7	LPT1	Yes	Note(1)
8	RTC	No	-
9	SCI	No	Note(2)
10	Free	Yes	-
11	Free	Yes	-
12	PS/2 Mouse	No	Note(1)
13	FPU	No	-
14	IDE0	No	Note(1)
15	IDE1	No	Note(1)

1 If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.

2 Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. Currently not free in Non-ACPI mode.

5.1.2 In APIC mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	-
1	Keyboard	No	-
2	Slave 8259	No	-
3	COM2	Yes	Note (1)
4	COM1	Yes	Note (1)
5	PCI/LPT2	Yes	-
6	Floppy Drive Controller	Yes	Note (1)
7	LPT1	Yes	Note (1)
8	RTC	No	-
9	SCI	No	Note (2)
10	COM3	No	Note (1)
11	COM4	No	Note (1)
12	PS/2 Mouse	Yes	Note (1)
13	FPU	No	-
14	IDE0	No	Note (1)
15	IDE1	No	Note (1)
16	PIRQ[A]	For PCI	PCI IRQ line 1 + Graphics controller + HD Audio Controller + secondary IDE
17	PIRQ[B]	For PCI	PCI IRQ line 2 + AC'97 Audio controller
18	PIRQ[C]	For PCI	PCI IRQ line 3 + USB UHCI controller #3 + SATA (native mode)
19	PIRQ[D]	For PCI	PCI IRQ line 4 + USB UHCI controller #2 + IDE (native mode)
20	PIRQ[E]	No	Lan Controller
21	PIRQ[F]	No	-
22	PIRQ[G]	No	-
23	PIRQ[H]	No	USB EHCI controller, USB UCHI controller #1

1 If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.

2 Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. Currently not free in Non-ACPI mode.

5.2 Direct Memory Access (DMA) Channels

DMA#	Used For	Available	Comment
0		No	-
1		No	-
2	FDC	No	If the “used-for” device is disabled in setup, the corresponding DMA channel is avaialble for other devices
3	LPT	No	Unavailable if LPT is used in ECP mode
4	Cascade	No	-
5		No	-
6		No	-
7		No	-

5.3 Memory Area

Upper Memory	Used For	Available	Comment
C0000h-CFFFFh	VGA BIOS	No	
D0000h-DFFFFh		Yes	LPC Bus or Shadow RAM
E0000h-EFFFFh	System BIOS	No	

5.4 I/O Address Map

Upper Memory	Used For	Available	Comment
480h-4BFh	Chipset	No	Always used by chipset
800h-87Fh	Chipset	No	Always used by chipset
A00h-AFFh	Chipset	No	Always used by chipset
1000h>	PCI	No	

5.5 External Inter-IC (I2C) Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
				2

5.6 System Management (SM) Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
10h	SMB Hoste	No	Do not use under any circumstances.	1
12h	SMART_Charger	No	Only be used by a SMB Charger	1
14h	SMART_Selector	No	Only be used by a SMB Selector or Manager	1
16h	SMART_Battery	No	Only be used by a SMB Battery	1
A0h	SPD	No		1
D2h	Clockgenerator	No	Do not use ander any circumstances	1

5.7 JILI I2C Bus

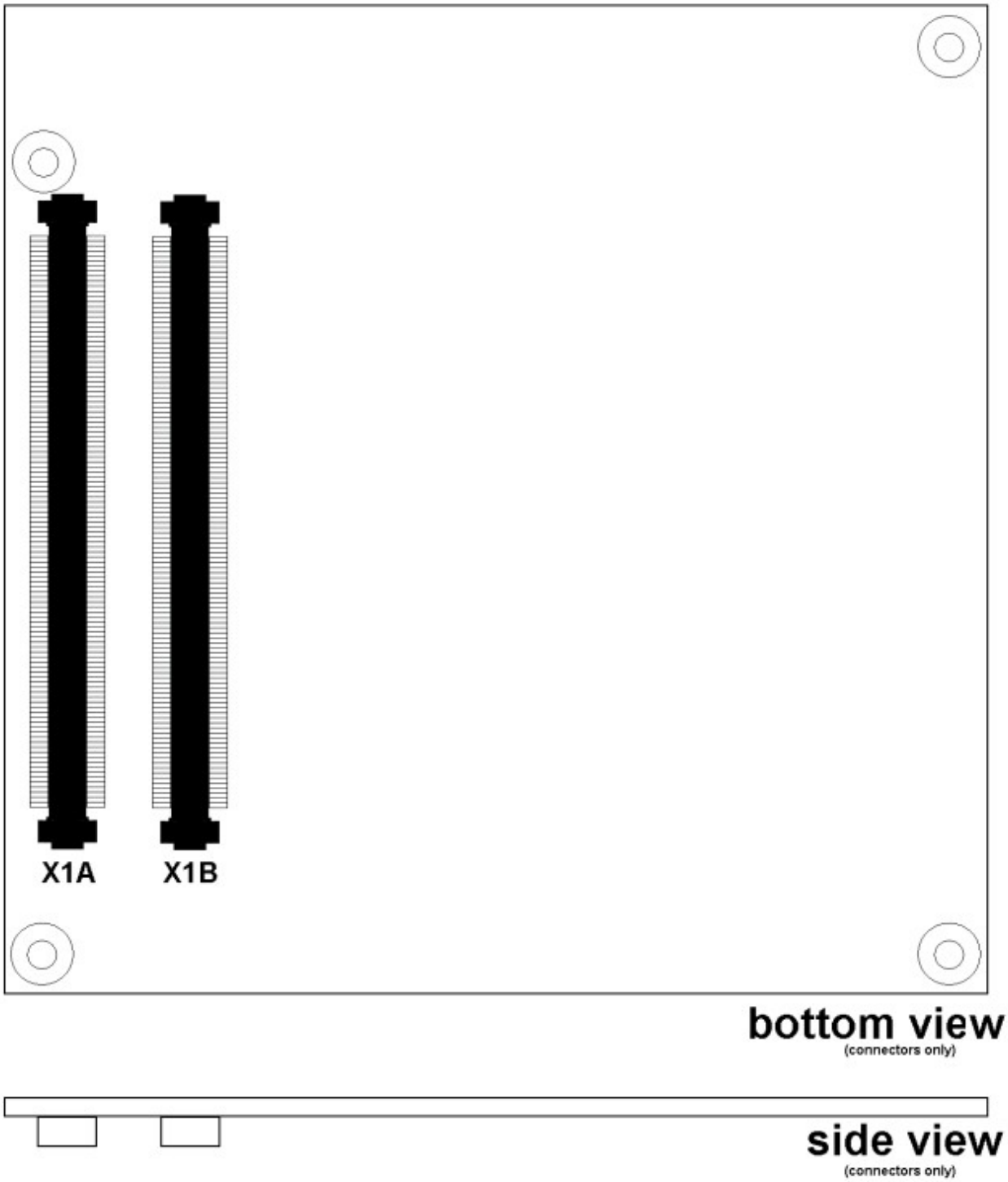
I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	DDC	No	EEPROM for JILI Data	3
62h	MAX5362	No	DAC for Backlight brightness	3

JIDA Bus Nr. 0 is for internal use only.

6 Connectors

The pinouts for Interface Connectors X1A and X1B are documented for convenient reference. Please see the COM Express™ Specification and COM Express™ Design Guide for detailed, design-level information.

6.1 Connector Location



6.2 Pinout List

6.2.1 General Signal Description

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1,8V Output
O-3,3	3,3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection

To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfills the fire-protection requirements of IEC/EN60950

6.2.2 Connector X1A Row A

Pin	Signal	Description	Type	Termination	Comment
A1	GND	Power Ground	PWR	-	-
A2	GBE0_MDI3-	GBE0_MDI3_N ; Ethernet Receive Data -	DP-I	-	-
A3	GBE0_MDI3+	GBE0_MDI3_P ; Ethernet Receive Data -	DP-I	-	-
A4	GBE0_LINK100#	GBE0_LINK100# ; Ethernet Speed LED	O-3,3	-	-
A5	GBE0_LINK1000#	GBE0_LINK1000# ; Ethernet Speed LED	O-3,3	-	-
A6	GBE0_MDI2-	GBE0_MDI2_N ; Ethernet Receive Data -	DP-I	-	-
A7	GBE0_MDI2+	GBE0_MDI2_P ; Ethernet Receive Data -	DP-I	-	-
A8	GBE0_LINK#	GBE0_LINK# ; LAN Link LED	OD	-	-
A9	GBE0_MDI1-	GBE0_MDI1_N ; Ethernet Receive Data -	DP-I	-	-
A10	GBE0_MDI1+	GBE0_MDI1_P ; Ethernet Receive Data +	DP-I	-	-
A11	GND	Power Ground	PWR	-	-
A12	GBE0_MDI0-	GBE0_MDI0_N ; Ethernet Transmit Data -	DP-O	-	-
A13	GBE0_MDI0+	GBE0_MDI0_P ; Ethernet Transmit Data +	DP-O	-	-
A14	GBE0_CTREF	GBE0_CTREF	O-1,8	-	-
A15	SUS_S3#	PM_SLP_S3_EXT#	O-3,3	-	-
A16	SATA0_TX+	SATA_TX0_P ; SATA 0 Transmit Data +	DP-O	-	-
A17	SATA0_TX-	SATA_TX0_N ; SATA 0 Transmit Data -	DP-O	-	-
A18	SUS_S4#	PM_SLP_S4_EXT#	O-3,3	-	-
A19	SATA0_RX+	SATA_RX0_P ; SATA 0 Receive Data +	DP-I	-	-
A20	SATA0_RX-	SATA_RX0_N ; SATA 0 Receive Data -	DP-I	-	-
A21	GND	Power Ground	PWR	-	-
A22	SATA2_TX+	SATA_TX2_P ; SATA 2 Transmit Data +	DP-O	-	-
A23	SATA2_TX-	SATA_TX2_N ; SATA 2 Transmit Data -	DP-O	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3,3	-	-
A25	SATA2_RX+	SATA_RX2_P ; SATA 2 Receive Data +	DP-I	-	-
A26	SATA2_RX-	SATA_RX2_N ; SATA 2 Receive Data -	DP-I	-	-
A27	BATLOW#	PM_BATLOW# ; Battery Low	I-3,3	PU 8k25 3,3V (S5)	-
A28	ATA_ACT#	ATA_LED# ; SATA LED	O-3,3	PU 15k in ICH7	-
A29	AC_SYNC	HDA_SYNC ; HD Audio Sync	O-3,3	PD 20k in ICH7	-
A30	AC_RST#	HDA_RST# ; HD Audio Reset	O-3,3	-	-
A31	GND	Power Ground	PWR	-	-
A32	AC_BITCLK	HDA_BITCLK ; HD Audio Clock	O-3,3	int. PD 20k in ICH7	-
A33	AC_SDOUT	HDA_SDOUT ; HD Audio Data	O-3,3	int. PD 20k in ICH7	-
A34	BIOS_DISABLE#	BIOS_DISABLE#	I-3,3	PU 10k 3,3V (S0)	-
A35	THRMTRIP#	EXT_THRMTRIP#	I/O-3,3	PU 10k 3,3V (S0)	-
A36	USB6-	USB6_N ; USB Data – Port6	DP-I/O	PD 15k in ICH7	-
A37	USB6+	USB6_P ; USB Data + Port6	DP-I/O	PD 15k in ICH7	-
A38	USB_6_7_OC#	USB_67_OC# ; USB OverCurrent Port 6/7	I-3,3	PU 10k 3,3V (S5)	-
A39	USB4-	USB4_N ; USB Data - Port4	DP-I/O	PD 15k in ICH7	-
A40	USB4+	USB4_P ; USB Data + Port4	DP-I/O	PD 15k in ICH7	-
A41	GND	Power Ground	PWR	-	-
A42	USB2-	USB2_N ; USB Data - Port2	DP-I/O	PD 15k in ICH7	-
A43	USB2+	USB2_P ; USB Data + Port2	DP-I/O	PD 15k in ICH7	-
A44	USB_2_3_OC#	USB_23_OC# ; USB OverCurrent Port 2/3	I-3,3	PU 10k 3,3V (S5)	-
A45	USB0-	USB0_N ; USB Data - Port0	DP-I/O	PD 15k in ICH7	-
A46	USB0+	USB0_P ; USB Data + Port0	DP-I/O	PD 15k in ICH7	-
A47	VCC_RTC	V_BAT	PWR 3V	-	-
A48	EXCD0_PERST#	EXCD0_PERST#;Express card reset	O-3,3	-	-
A49	EXCD0_CPPE#	EXCD0_CPPE# ; capable c. request	I-3,3	PU 8k25 3,3V (S5)	-
A50	LPC_SERIRQ	LPC_SERIRQ ; Serial Interrupt Request	IO-3,3	PU 8k25 3,3V (S0)	-
A51	GND	Power Ground	PWR	-	-
A52	PCIE_TX5+	nc	Nc	-	-
A53	PCIE_TX5-	nc	Nc	-	-
A54	GPI0	EXT_GPI0 ; General Purpose Input 0	I-3,3	PU 10k 3,3V (S0)	-
A55	PCIE_TX4+	nc	nc	-	-
A56	PCIE_TX4-	nc	nc	-	-
A57	GND	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCI Express lane 3 + Transmit	DP-O	-	Only available if no LAN is equipped.
A59	PCIE_TX3-	PCI Express lane 3 - Transmit	DP-O	-	Only available if no LAN is equipped.
A60	GND	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCI Express lane 2 + Transmit	DP-O	-	-
A62	PCIE_TX2-	PCI Express lane 2 - Transmit	DP-O	-	-
A63	GPI1	EXT_GPI1 ; General Purpose Input 1	I-3,3	PU 10k 3,3V (S0)	-

A64	PCIE_TX1+	PCI Express lane 1 + Transmit	DP-O	-	-
A65	PCIE_TX1-	PCI Express lane 1 - Transmit	DP-O	-	-
A66	GND	Power Ground	PWR	-	-
A67	GPI2	EXT_GPI2 ; General Purpose Input 2	I-3,3	PU 10k 3,3V (S0)	-
A68	PCIE_TX0+	PCI Express lane 0 + Transmit	DP-O	-	-
A69	PCIE_TX0-	PCI Express lane 0 - Transmit	DP-O	-	-
A70	GND	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS_A_DATA0_P ; LVDS Channel A Data0+	DP-O	-	-
A72	LVDS_A0-	LVDS_A_DATA0_N ; LVDS Channel A Data0-	DP-O	-	-
A73	LVDS_A1+	LVDS_A_DATA1_P ; LVDS Channel A Data1+	DP-O	-	-
A74	LVDS_A1-	LVDS_A_DATA1_N ; LVDS Channel A Data1-	DP-O	-	-
A75	LVDS_A2+	LVDS_A_DATA2_P ; LVDS Channel A Data2+	DP-O	-	-
A76	LVDS_A2-	LVDS_A_DATA2_N ; LVDS Channel A Data2-	DP-O	-	-
A77	LVDS_VDD_EN	LVDS_VDD_EN ; LVDS Panel Power Control	O-3,3	PD 100k	-
A78	LVDS_A3+	nc	nc	-	-
A79	LVDS_A3-	nc	nc	-	-
A80	GND	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_A_CLK_P ; LVDS Channel A Clock+	DP-O	-	-
A82	LVDS_A_CK-	LVDS_A_CLK_N ; LVDS Channel A Clock-	DP-O	-	-
A83	LVDS_I2C_CK	LVDS_DDC_CLK ; JILI I2C Clock	I/O-3,3	PU 2k21 3,3V (s0)	-
A84	LVDS_I2C_DAT	LVDS_DDC_DATA ; JILI I2C Data	I/O-3,3	PU 2k21 3,3V (s0)	-
A85	GPI3	EXT_GPI3 ; General Purpose Input 3	I-3,3	PU 10k 3,3V (S0)	-
A86	KBD_RST#	KBD_RST# ; Keyboard Reset	I-3,3	PU 10k 3,3V (S0)	-
A87	KBD_A20GATE	KBD_A20GATE	I-3,3	PU 10k 3,3V (S0)	-
A88	PCIE0_CK_REF+	CLK_PCIE_CON_P	DP-O	-	-
A89	PCIE0_CK_REF-	CLK_PCIE_CON_N	DP-O	-	-
A90	GND	Power Ground	PWR	-	-
A91	RSVD	n.c.	Nc	-	-
A92	RSVD	n.c.	Nc	-	-
A93	GPO0	EXT_GPO0 ; General Purpose Output 0	O-3,3	PD 10k	-
A94	RSVD	n.c.	Nc	-	-
A95	RSVD	n.c.	Nc	-	-
A96	GND	Power Ground	PWR	-	-
A97	VCC_12V	12V VCC	PWR	-	8.5-18V
A98	VCC_12V	12V VCC	PWR	-	8.5-18V
A99	VCC_12V	12V VCC	PWR	-	8.5-18V
A100	GND	Power Ground	PWR	-	-
A101	VCC_12V	12V VCC	PWR	-	8.5-18V
A102	VCC_12V	12V VCC	PWR	-	8.5-18V
A103	VCC_12V	12V VCC	PWR	-	8.5-18V
A104	VCC_12V	12V VCC	PWR	-	8.5-18V
A105	VCC_12V	12V VCC	PWR	-	8.5-18V
A106	VCC_12V	12V VCC	PWR	-	8.5-18V
A107	VCC_12V	12V VCC	PWR	-	8.5-18V
A108	VCC_12V	12V VCC	PWR	-	8.5-18V
A109	VCC_12V	12V VCC	PWR	-	8.5-18V
A110	GND	Power Ground	PWR	-	-

6.2.3 Connector X1A Row B

Pin	Signal	Description	Type	Termination	Comment
B1	GND	Power Ground	PWR	-	-
B2	GBE0_ACT	GBE0_ACT# ; Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC_FRAME# ; LPC Frame Indicator	I-3,3	-	-
B4	LPC_AD0	LPC_AD0 ; LPC Adress & DATA Bus	I/O-3,3	PU 20k in ICH7	-
B5	LPC_AD1	LPC_AD1 ; LPC Adress & DATA Bus	I/O-3,3	PU 20k in ICH7	-
B6	LPC_AD2	LPC_AD2 ; LPC Adress & DATA Bus	I/O-3,3	PU 20k in ICH7	-
B7	LPC_AD3	LPC_AD3 ; LPC Adress & DATA Bus	I/O-3,3	PU 20k in ICH7	-
B8	LPC_DRQ0#	LPC_DRQ#0 ; LPC Request 0	I-3,3	PU 20k in ICH7	-
B9	LPC_DRQ1#	LPC_DRQ#1 ; LPC Request 1	I-3,3	PU 20k in ICH7	-
B10	LPC_CLK	CLK_LPC_33M_EXT ; 33MHz LPC clock	O-3,3	-	-
B11	GND	Power Ground	PWR	-	-
B12	PWRBTN#	EXT_PWRBTN# ; Power Button	I-3,3	PU 10k 3,3V (S5)	-
B13	SMB_CK	SMB_CLK_EXT ; SMBUS Clock	O-3,3	PU 2k2 3,3V (S5)	-
B14	SMB_DAT	SMB_DATA_EXT ; SMBUS Data	IO-3,3	PU 2k2 3,3V (S5)	-
B15	SMB_ALERT#	SMB_ALERT# ; SMBUS Interrupt	IO-3,3	PU 1k0 3,3V (S5)	-
B16	SATA1_TX+	SATA_TX1_P ; SATA 1 Transmit Data +	DP-O	-	-
B17	SATA1_TX-	SATA_TX1_N ; SATA 1 Transmit Data -	DP-O	-	-
B18	SUS_STAT#	PM_SUS_ STAT#	O-3,3	-	-
B19	SATA1_RX+	SATA_RX1_P ; SATA 1 Receive Data +	DP-I	-	-
B20	SATA1_RX-	SATA_RX1_N ; SATA 1 Receive Data -	DP-I	-	-
B21	GND	Power Ground	PWR	-	-
B22	SATA3_TX+	nc	nc	-	-
B23	SATA3_TX-	nc	nc	-	-
B24	PWR_OK	EXT_PWR_OK ; Power OK	I-3,3	-	-
B25	SATA3_RX+	nc	nc	-	-
B26	SATA3_RX-	nc	nc	-	-
B27	WDT	WDT ; Watch Dog Timer	O-3,3	-	-
B28	AC_SDIN2	HDA_SDIN2_ICH ; HD Audio Serial Input Data 2	I-3,3	PD 20k in ICH7	-
B29	AC_SDIN1	HDA_SDIN1_ICH ; HD Audio Serial Input Data 1	I-3,3	PD 20k in ICH7	-
B30	AC_SDIN0	HDA_SDIN0_ICH ; HD Audio Serial Input Data 0	I-3,3	PD 20k in ICH7	-
B31	GND	Power Ground	PWR	-	-
B32	SPKR	HDA_SPKR ; Speaker	O-3,3	PD 20k in ICH7	-
B33	I2C_CK	I2C_CLK_EXT ; I2C clock	O-3,3	PU 2k21 3,3V (S0)	-
B34	I2C_DAT	I2C_DATA_EXT ; I2C data	I/O-3,3	PU 2k21 3,3V (S0)	-
B35	THRM#	PM_THRM# ; Over Temperature	O-3,3	-	-
B36	USB7-	USB7_N ; USB Data – Port7	DP-I/O	PD 15k in ICH7	-
B37	USB7+	USB7_P ; USB Data + Port7	DP-I/O	PD 15k in ICH7	-
B38	USB_4_5_OC#	USB_45_OC# ; USB OverCurrent Port 4/5	I-3,3	PU 10k 3,3V (S5)	-
B39	USB5-	USB5_N ; USB Data – Port5	DP-I/O	PD 15k in ICH7	-
B40	USB5+	USB5_P ; USB Data + Port5	DP-I/O	PD 15k in ICH7	-
B41	GND	Power Ground	PWR	-	-
B42	USB3-	USB3_N ; USB Data – Port3	DP-I/O	PD 15k in ICH7	-
B43	USB3+	USB3_P ; USB Data + Port3	DP-I/O	PD 15k in ICH7	-
B44	USB_0_1_OC#	USB_01_OC# ; USB OverCurrent Port 0/1	I-3,3	PU 10k 3,3V (S5)	-
B45	USB1-	USB1_N ; USB Data – Port1	DP-I/O	PD 15k in ICH7	-
B46	USB1+	USB1_P ; USB Data + Port1	DP-I/O	PD 15k in ICH7	-
B47	EXCD1_PERST#	EXCD1_PERST# ; Express card reset	O-3,3	-	-
B48	EXCD1_CPPE#	EXCD1_CPPE# ; capable c. request	I-3,3	PU 8k25 3,3V (S0)	-
B49	SYS_RESET#	EXT_SYS_RESET# ; Reset Input	I-3,3	PU 10k 3,3V (S5)	-
B50	CB_RESET#	CB_RESET# ; Carrier board Reset	O-3,3	-	-
B51	GND	Power Ground	PWR	-	-
B52	PCIE_RX5+	nc	Nc	-	-
B53	PCIE_RX5-	nc	Nc	-	-
B54	GPO1	EXT_GPO1 ; General Purpose Output 1	O-3,3	-	-
B55	PCIE_RX4+	nc	nc	-	-
B56	PCIE_RX4-	nc	nc	-	-
B57	GPO2	EXT_GPO2 ; General Purpose Output 2	O-3,3	-	-
B58	PCIE_RX3+	PCI Express lane 3 + Recieve	DP-I	-	only available if no LAN
B59	PCIE_RX3-	PCI Express lane 3 - Recieve	DP-I	-	only available if no LAN
B60	GND	Power Ground	PWR	-	-
B61	PCIE_RX2+	PCI Express lane 2 + Recieve	DP-I	-	-
B62	PCIE_RX2-	PCI Express lane 2 - Recieve	DP-I	-	-
B63	GPO3	EXT_GPO3 ; General Purpose Output 3	O-3,3	-	-
B64	PCIE_RX1+	PCI Express lane 1 + Recieve	DP-I	-	-

B65	PCIE_RX1-	PCI Express lane 1 - Recieve	DP-I	-	-
B66	WAKE0#	PCIE_WAKE#	IO-3,3	PU 1k0 3,3V (S5)	-
B67	WAKE1#	WAKE1#	I-3,3	PU 10k 3,3V (S5)	-
B68	PCIE_RX0+	PCI Express lane 0 + Recieve	DP-I	-	-
B69	PCIE_RX0-	PCI Express lane 0 - Recieve	DP-I	-	-
B70	GND	Power Ground	PWR	-	-
B71	LVDS_B0+	LVDS_B_DATA0_P ; LVDS Channel B Data0+	DP-O	-	-
B72	LVDS_B0-	LVDS_B_DATA0_N ; LVDS Channel B Data0-	DP-O	-	-
B73	LVDS_B1+	LVDS_B_DATA1_P ; LVDS Channel B Data1+	DP-O	-	-
B74	LVDS_B1-	LVDS_B_DATA1_N ; LVDS Channel B Data1-	DP-O	-	-
B75	LVDS_B2+	LVDS_B_DATA2_P ; LVDS Channel B Data2+	DP-O	-	-
B76	LVDS_B2-	LVDS_B_DATA2_N ; LVDS Channel B Data2-	DP-O	-	-
B77	LVDS_B3+	nc	nc	-	-
B78	LVDS_B3-	nc	nc	-	-
B79	LVDS_BKLT_EN	LVDS_BKLT_CTRL ; Panel Backlight ON	O-3,3	PD 100k	-
B80	GND	Power Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_B_CLK_P ; LVDS Channel B Clock+	DP-O	-	-
B82	LVDS_B_CK-	LVDS_B_CLK_N ; LVDS Channel B Clock-	DP-O	-	-
B83	LVDS_BKLT_CTRL	LVDS_BKLT_CTRL ; Backlight Brightness Contr.	O-3,3	PD 100k	-
B84	VCC_5V_SBY	+V_STBY_ETX ; 5V Standby	PWR 5V (S5)	-	-
B85	VCC_5V_SBY	+V_STBY_ETX ; 5V Standby	PWR 5V (S5)	-	-
B86	VCC_5V_SBY	+V_STBY_ETX ; 5V Standby	PWR 5V (S5)	-	-
B87	VCC_5V_SBY	+V_STBY_ETX ; 5V Standby	PWR 5V (S5)	-	-
B88	RSVD	n.c.	nc	-	-
B89	VGA_RED	CRT_RED ; Analog Video RGB-RED	OA	PD 150R	-
B90	GND	Power Ground	PWR	-	-
B91	VGA_GRN	CRT_GREEN ; Analog Video RGB-GREEN	OA	PD 150R	-
B92	VGA_BLU	CRT_BLUE ; Analog Video RGB-BLUE	OA	PD 150R	-
B93	VGA_HSYNC	CRT_HSYNC ; Analog Video H-Sync	O-3,3	-	-
B94	VGA_VSYNC	CRT_VSYNC ; Analog Video V-Sync	O-3,3	-	-
B95	VGA_I2C_CK	CRT_DDC_CLK ; Display Data Channel Clock	I/O-5	PU 2k21 5V (S0)	-
B96	VGA_I2C_DAT	CRT_DDC_DATA ; Display Data Channel Data	I/O-5	PU 2k21 5V (S0)	-
B97	TV_DAC_A	TV_DACA_CVBS ; Composite CVBS	OA	PD 150R	-
B98	TV_DAC_B	TV_DADB_Y ; TV Luminance Signal	OA	PD 150R	-
B99	TV_DAC_C	TV_DADC_C ; TV Chrominance Signal	OA	PD 150R	-
B100	GND	Power Ground	PWR	-	-
B101	VCC_12V	12V VCC	PWR	-	8.5-18V
B102	VCC_12V	12V VCC	PWR	-	8.5-18V
B103	VCC_12V	12V VCC	PWR	-	8.5-18V
B104	VCC_12V	12V VCC	PWR	-	8.5-18V
B105	VCC_12V	12V VCC	PWR	-	8.5-18V
B106	VCC_12V	12V VCC	PWR	-	8.5-18V
B107	VCC_12V	12V VCC	PWR	-	8.5-18V
B108	VCC_12V	12V VCC	PWR	-	8.5-18V
B109	VCC_12V	12V VCC	PWR	-	8.5-18V
B110	GND	Power Ground	PWR	-	-

6.2.4 Connector X1B Row C

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	I/O-5T	-	-
C3	IDE_D6	IDE Data Bus	I/O-5T	-	-
C4	IDE_D3	IDE Data Bus	I/O-5T	-	-
C5	IDE_D15	IDE Data Bus	I/O-5T	-	-
C6	IDE_D8	IDE Data Bus	I/O-5T	-	-
C7	IDE_D9	IDE Data Bus	I/O-5T	-	-
C8	IDE_D2	IDE Data Bus	I/O-5T	-	-
C9	IDE_D13	IDE Data Bus	I/O-5T	-	-
C10	IDE_D1	IDE Data Bus	I/O-5T	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	I/O-5T	-	-
C13	IDE_IORDY	IDE I/O Ready	I/O-5T	PU 4k7 3,3V (S0)	-
C14	IDE_IOR#	IDE I/O Read	I/O-3,3	-	-
C15	PCI_PME#	PCI Power Management Event	I/O-3,3	-	-
C16	PCI_GNT2#	PCI Bus Grant 2	O-3,3	PU 20k in ICH7	-
C17	PCI_REQ2#	PCI Bus Request 2	I-5T	PU 8k2 3,3V (S0)	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3,3	PU 20k in ICH7	-
C19	PCI_REQ1#	PCI Bus Request 1	I-5T	PU 8k2 3,3V (S0)	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3,3	PU 20k in ICH7	-
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-5T	PU 8k2 3,3V (S0)	-
C23	PCI_RST#	PCI Bus Reset	O-3,3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	I/O-5T	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	I/O-5T	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	I/O-5T	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	I/O-5T	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	I/O-5T	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	I/O-5T	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	I/O-5T	-	-
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	I/O-5T	-	-
C33	PCI_C/BE1#	PCI Bus Cmd Byte enables 1	I/O-5T	-	-
C34	PCI_PERR#	PCI Bus Grant Error	I/O-5T	PU 8k2 3,3V (S0)	-
C35	PCI_LOCK#	PCI Bus Lock	I/O-5T	PU 8k2 3,3V (S0)	-
C36	PCI_DEVSEL#	PCI Bus Device Select	I/O-5T	PU 8k2 3,3V (S0)	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	I/O-5T	PU 8k2 3,3V (S0)	-
C38	PCI_C/BE2#	PCI Bus Cmd Byte enables 2	I/O-5T	-	-
C39	PCI_AD17	PCI Adress & Data Bus line	I/O-5T	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	I/O-5T	-	-
C41	GND	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	I/O-5T	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	I/O-5T	-	-
C44	PCI_C/BE3#	PCI Bus Cmd Byte enables 3	I/O-5T	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	I/O-5T	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	I/O-5T	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	I/O-5T	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	I/O-5T	-	-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-5T	PU 8k2 3,3V (S0)	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-5T	PU 8k2 3,3V (S0)	-
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	SDVO_TV_CLKIN_P	DP-I	-	-
C53	PEG_RX0-	SDVO_TV_CLKIN_N	DP-I	-	-
C54	TYPE0#	n.c. for type 2 module	nc	-	-
C55	PEG_RX1+	SDVO_INT_P	DP-I	-	-
C56	PEG_RX1-	SDVO_INT_N	DP-I	-	-
C57	TYPE1#	n.c. for type 2 module	nc	-	-
C58	PEG_RX2+	SDVO_FLDSTAL_P	DP-I	-	-
C59	PEG_RX2-	SDVO_FLDSTAL_N	DP-I	-	-
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	n.c.	nc	-	-
C62	PEG_RX3-	n.c.	nc	-	-
C63	RSVD	n.c.	nc	-	-
C64	RSVD	n.c.	nc	-	-

C65	PEG_RX4+	n.c.	nc	-	-
C66	PEG_RX4-	n.c.	nc	-	-
C67	RSVD	n.c.	nc	-	-
C68	PEG_RX5+	n.c.	nc	-	-
C69	PEG_RX5-	n.c.	nc	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	n.c.	nc	-	-
C72	PEG_RX6-	n.c.	nc	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	I/O-3,3	-	-
C74	PEG_RX7+	n.c.	nc	-	-
C75	PEG_RX7-	n.c.	nc	-	-
C76	GND	Power Ground	PWR	-	-
C77	RSVD	n.c.	nc	-	-
C78	PEG_RX8+	n.c.	nc	-	-
C79	PEG_RX8-	n.c.	nc	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	n.c.	nc	-	-
C82	PEG_RX9-	n.c.	nc	-	-
C83	RSVD	n.c.	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	n.c.	nc	-	-
C86	PEG_RX10-	n.c.	nc	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	n.c.	nc	-	-
C89	PEG_RX11-	n.c.	nc	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	n.c.	nc	-	-
C92	PEG_RX12-	n.c.	nc	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	n.c.	nc	-	-
C95	PEG_RX13-	n.c.	nc	-	-
C96	GND	Power Ground	PWR	-	-
C97	RSVD	n.c.	nc	-	-
C98	PEG_RX14+	n.c.	nc	-	-
C99	PEG_RX14-	n.c.	nc	-	-
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	n.c.	nc	-	-
C102	PEG_RX15-	n.c.	nc	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	8.5-18V
C106	VCC_12V	12V VCC	PWR	-	8.5-18V
C105	VCC_12V	12V VCC	PWR	-	8.5-18V
C107	VCC_12V	12V VCC	PWR	-	8.5-18V
C108	VCC_12V	12V VCC	PWR	-	8.5-18V
C109	VCC_12V	12V VCC	PWR	-	8.5-18V
C110	GND	Power Ground	PWR	-	-

6.2.5 Connector X1B Row D

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	I/O-5T	-	-
D3	IDE_D10	IDE Data Bus	I/O-5T	-	-
D4	IDE_D11	IDE Data Bus	I/O-5T	-	-
D5	IDE_D12	IDE Data Bus	I/O-5T	-	-
D6	IDE_D4	IDE Data Bus	I/O-5T	-	-
D7	IDE_D0	IDE Data Bus	I/O-5T	-	-
D8	IDE_REQ	IDE Data Bus	I/O-5T	-	-
D9	IDE_IOW#	IDE IO Write	O-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3,3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-5T	PD 8k25	-
D13	IDE_A0	IDE Adress Bus	O-3,3	-	-
D14	IDE_A1	IDE Adress Bus	O-3,3	-	-
D15	IDE_A2	IDE Adress Bus	O-3,3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3,3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	O-3,3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O-3,3	-	-
D19	PCI_GNT3#	PCI Bus Grant 3	O-3,3	PU 20k in ICH7	int. PU 20k in ICH9 (if PCIRST#=0 AND PWROK=1)
D20	PCI_REQ3#	PCI Bus Reqest 0	I-5T	PU 8k2 3,3V (S0)	-
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	I/O-5T	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	I/O-5T	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	I/O-5T	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	I/O-5T	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	I/O-5T	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	I/O-5T	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	I/O-5T	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	I/O-5T	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	I/O-5T	-	-
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	I/O-5T	-	-
D33	PCI_SERR#	PCI Bus System Error	I/O-5T	PU 8k2 3,3V (S0)	-
D34	PCI_STOP#	PCI Bus Stop	I/O-5T	PU 8k2 3,3V (S0)	-
D35	PCI_TRDY#	PCI Bus Target Ready	I/O-5T	PU 8k2 3,3V (S0)	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	I/O-5T	PU 8k2 3,3V (S0)	-
D37	PCI_AD16	PCI Adress & Data Bus line	I/O-5T	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	I/O-5T	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	I/O-5T	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	I/O-5T	-	-
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	I/O-5T	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	I/O-5T	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	I/O-5T	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	I/O-5T	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-5T	PU 8k2 3,3V (S0)	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-5T	PU 8k2 3,3V (S0)	-
D48	PCI_CLKRUN#	PCI Clock Run	I-5T	PU 8k25 3,3V (S0)	-
D49	PCI_M66EN	n.c.	nc	-	-
D50	PCI_CLK	CLK_PCI_33M_EXT ; PCI Clock 33MHz	O-3,3	-	-
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	SDVPB_RED_P	DP-O	-	-
D53	PEG_TX0-	SDVPB_RED_N	DP-O	-	-
D54	PEG_LANE_RV#	n.c.	nc	-	-
D55	PEG_TX1+	SDVPB_GREEN_P	DP-O	-	-
D56	PEG_TX1-	SDVPB_GREEN_N	DP-O	-	-
D57	TYPE2#	n.c. for type 2 module	nc	-	-
D58	PEG_TX2+	SDVPB_BLUE_P	DP-O	-	-
D59	PEG_TX2-	SDVPB_BLUE_N	DP-O	-	-
D60	GND	Power Ground	PWR	-	-
D61	PEG_TX3+	SDVPB_CLK_P	DP-O	-	-
D62	PEG_TX3-	SDVPB_CLK_N	DP-O	-	-
D63	RSVD	-	nc	-	-

D64	RSVD	-	nc	-	-
D65	PEG_TX4+	n.c.	nc	-	-
D66	PEG_TX4-	n.c.	nc	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	n.c.	nc	-	-
D69	PEG_TX5-	n.c.	nc	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	n.c.	nc	-	-
D72	PEG_TX6-	n.c.	nc	-	-
D73	SDVO_CLK	SDVO_CTRLCLK I	O-3,3	-	-
D74	PEG_TX7+	n.c.	nc	-	-
D75	PEG_TX7-	n.c.	nc	-	-
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE_CBLID# ; IDE cable type detect	I/O-3,3	PD 10k	-
D78	PEG_TX8+	n.c.	nc	-	-
D79	PEG_TX8-	n.c.	nc	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	n.c.	nc	-	-
D82	PEG_TX9-	n.c.	nc	-	-
D83	RSVD	n.c.	nc -	-	-
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	n.c.	nc	-	-
D86	PEG_TX10-	n.c.	nc	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX11+	n.c.	nc	-	-
D89	PEG_TX11-	n.c.	nc	-	-
D90	GND	Power Ground	PWR	-	-
D91	PEG_TX12+	n.c.	nc	-	-
D92	PEG_TX12-	n.c.	nc	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	n.c.	nc	-	-
D95	PEG_TX13-	n.c.	nc	-	-
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE#	n.c.	nc	PU 10k 3,3V (S0)	-
D98	PEG_TX14+	n.c.	nc	-	-
D99	PEG_TX14-	n.c.	nc	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	n.c.	nc	-	-
D102	PEG_TX15-	n.c.	nc	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	8.5-18V
D105	VCC_12V	12V VCC	PWR	-	8.5-18V
D106	VCC_12V	12V VCC	PWR	-	8.5-18V
D107	VCC_12V	12V VCC	PWR	-	8.5-18V
D108	VCC_12V	12V VCC	PWR	-	8.5-18V
D109	VCC_12V	12V VCC	PWR	-	8.5-18V
D110	GND	Power Ground	PWR	-	-

The termination resistors in these tables are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

7 BIOS Operation

The module is equipped with AMI® CORE8 BIOS, which is located in an onboard SPI/LPC flash memory. You can update the BIOS using a Flash utility.

7.1 Determining the BIOS Version

To determine the AMI® BIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

» AMIBIOS © 2006 American Megatrends, Inc.

» BIOS Date: mm/dd/yyyy hh:mm:ss Ver: xx.xx.xx

» Kontron® BIOS Version <UNP1RXXX

» Copyright 2002-2011 Kontron Embedded Modules GmbH

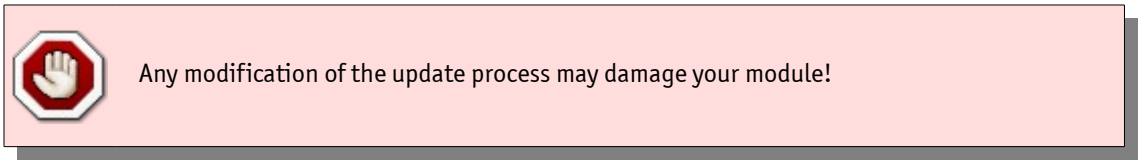
7.2 BIOS Update

Kontron provides continous BIOS updates for Computer-on-Modules. The updates are provided for download on http://emdcustomersection.kontron.com with a detailed change description within the according Product Change Notification (PCN). Please register for EMD Customer Section to get access to BIOS downloads and PCN service.

Modules with BIOS Region/Setup only inside the flash can be updated with AFU utilities (usually 1-3MB BIOS binary file size) directly. Modules with Intel® Management Engine, Ethernet, Flash Descriptor and other options additionally to the BIOS Region (usually 4-8MB BIOS binary file size) requires a different update process with Intel Flash Utility FPT and a wrapper to backup and restore configurations and the MAC address. Therefore it is strongly recommended to use the batch file inside the BIOS download package available on EMD Customer Section.

» Boot the module to DOS/EFI Shell with access to the BIOS image and Firmware Update Utility provided on EMD Customer Section

» Execute Flash.bat in DOS or Flash.nsh in EFI Shell



7.3 Setup Guide

The AMIBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

Functional keystrokes in POST:

Key	Function
DEL	Enter Setup
F2	Enter Setup
F11	Boot Menu
CTRL+HOME	Initiate BIOS Recovery

7.3.1 Start AMI® BIOS Setup Utility

To start the AMI® BIOS setup utility, press <DEL> when the following string appears during bootup.

Press <DEL> to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (►) marks all submenus.

Item Specific Help Window

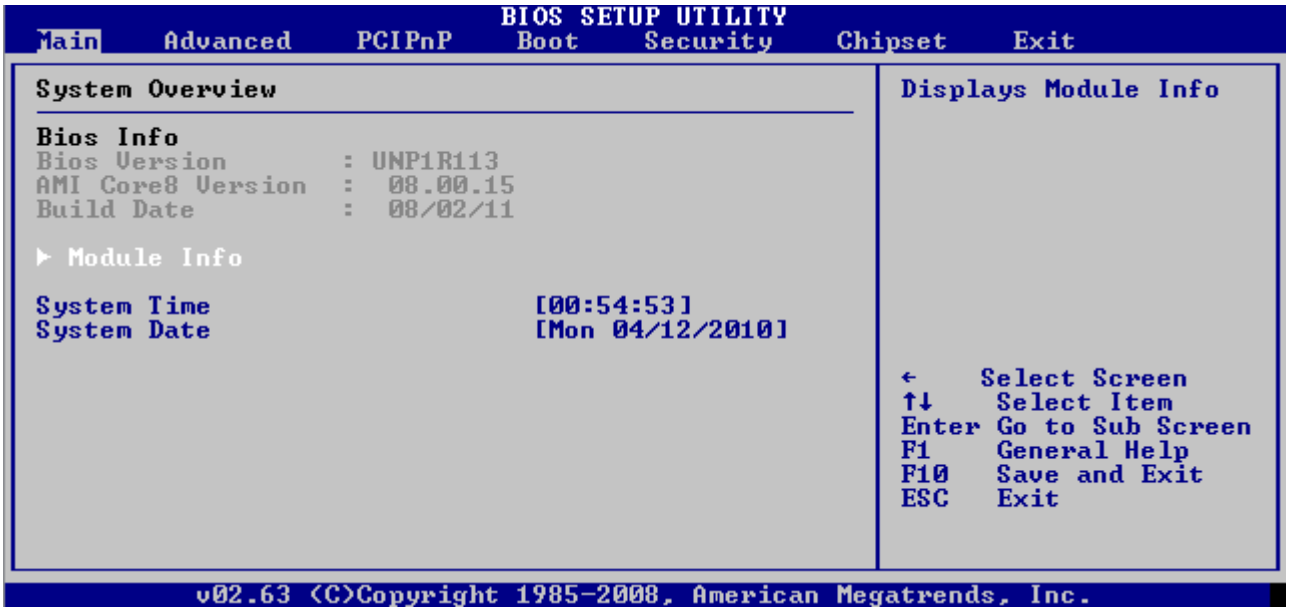
The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

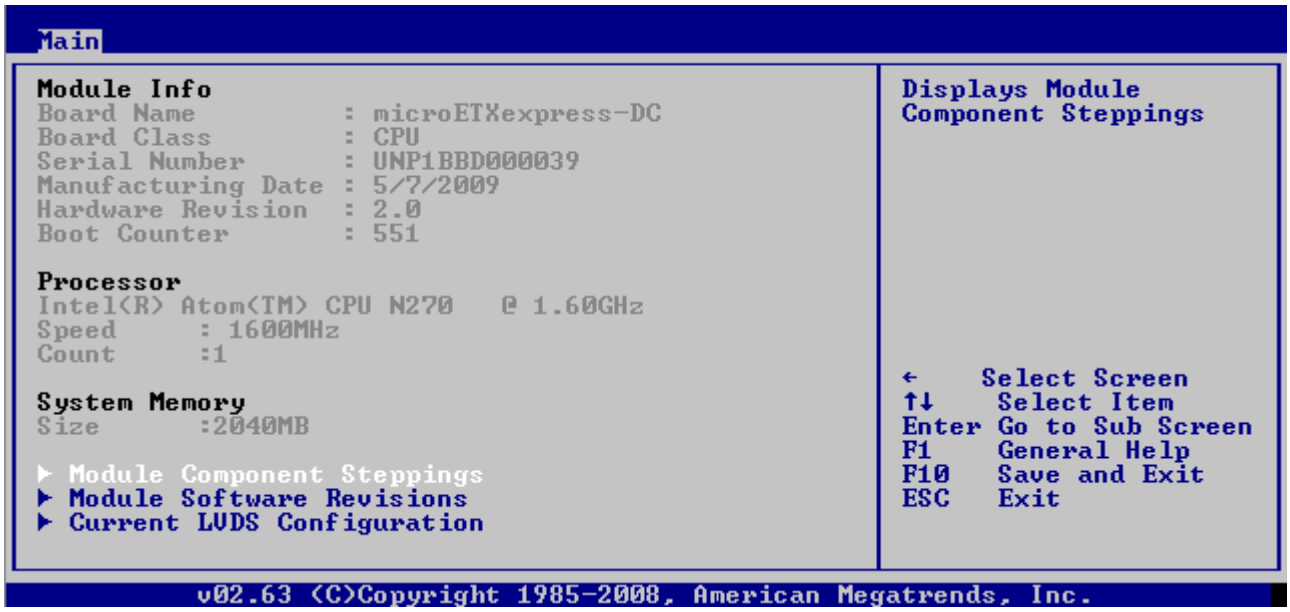
7.4 BIOS Setup

7.4.1 Main Menu

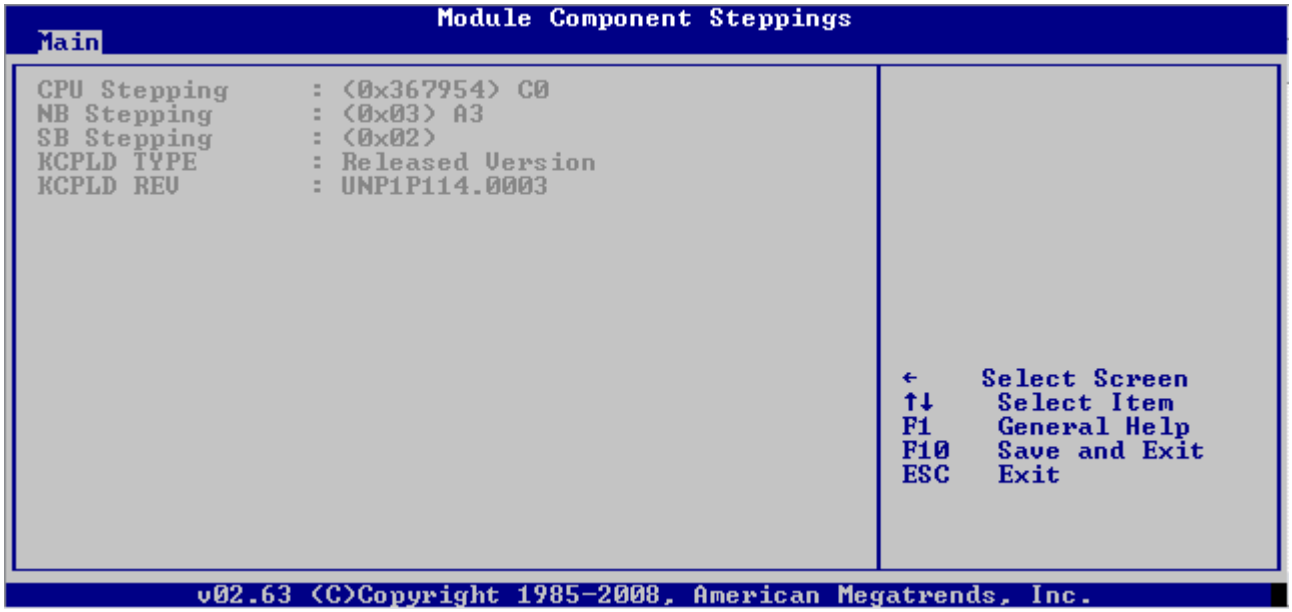


Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field

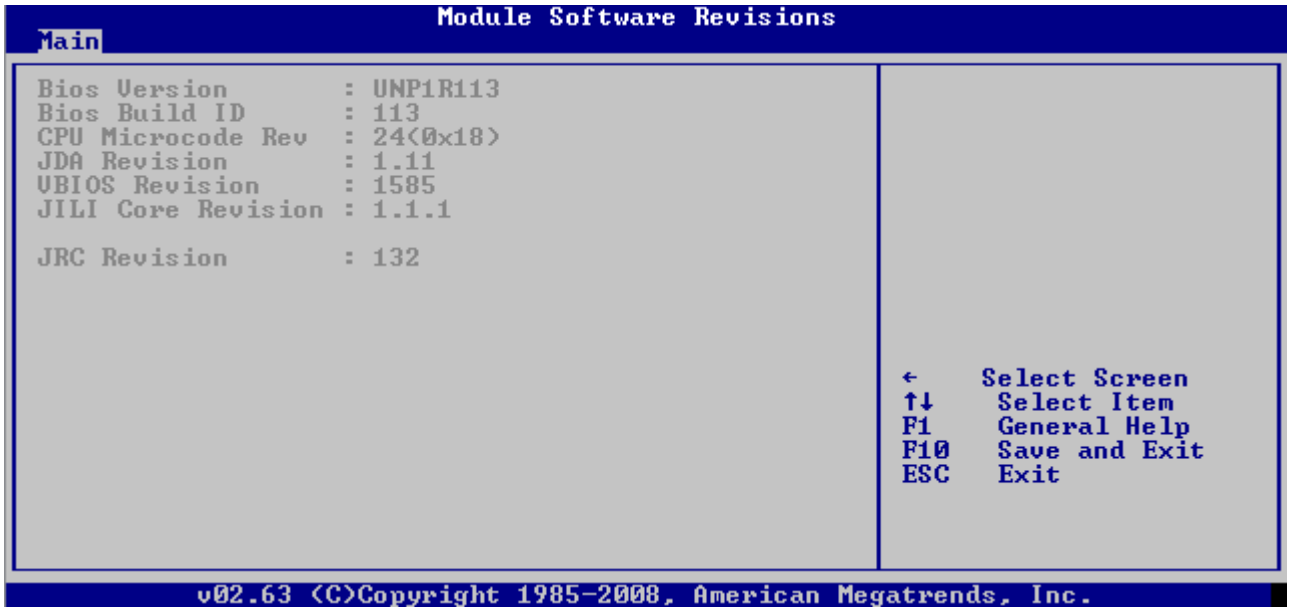
7.4.2 Module Info



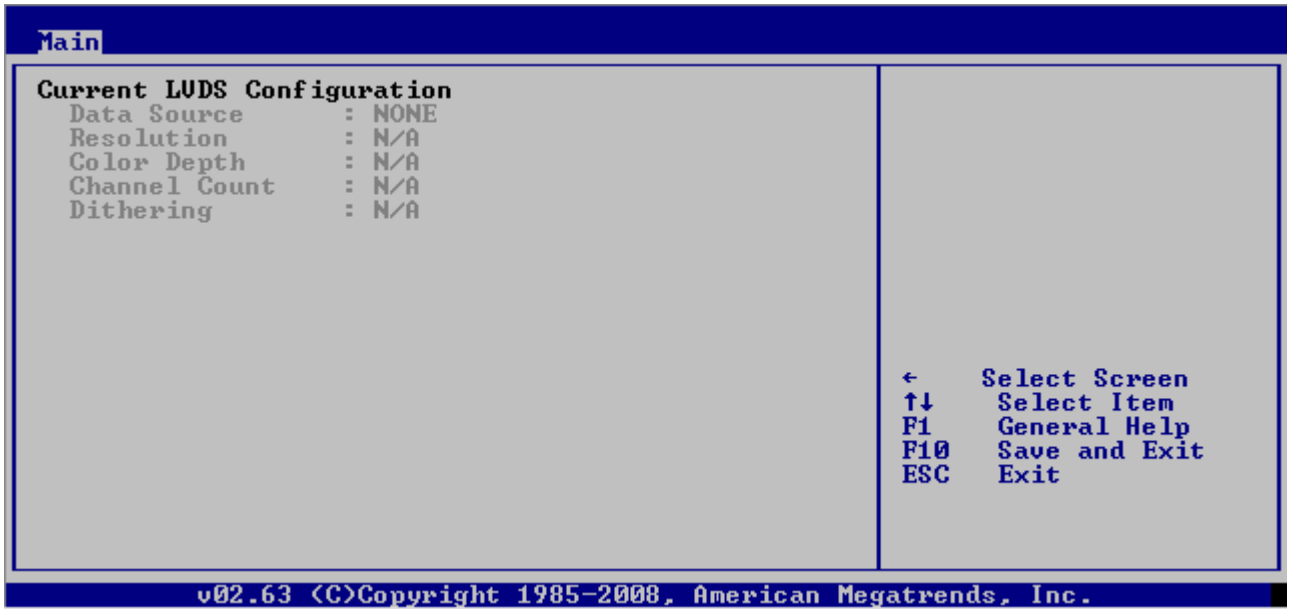
Module Component Steppings



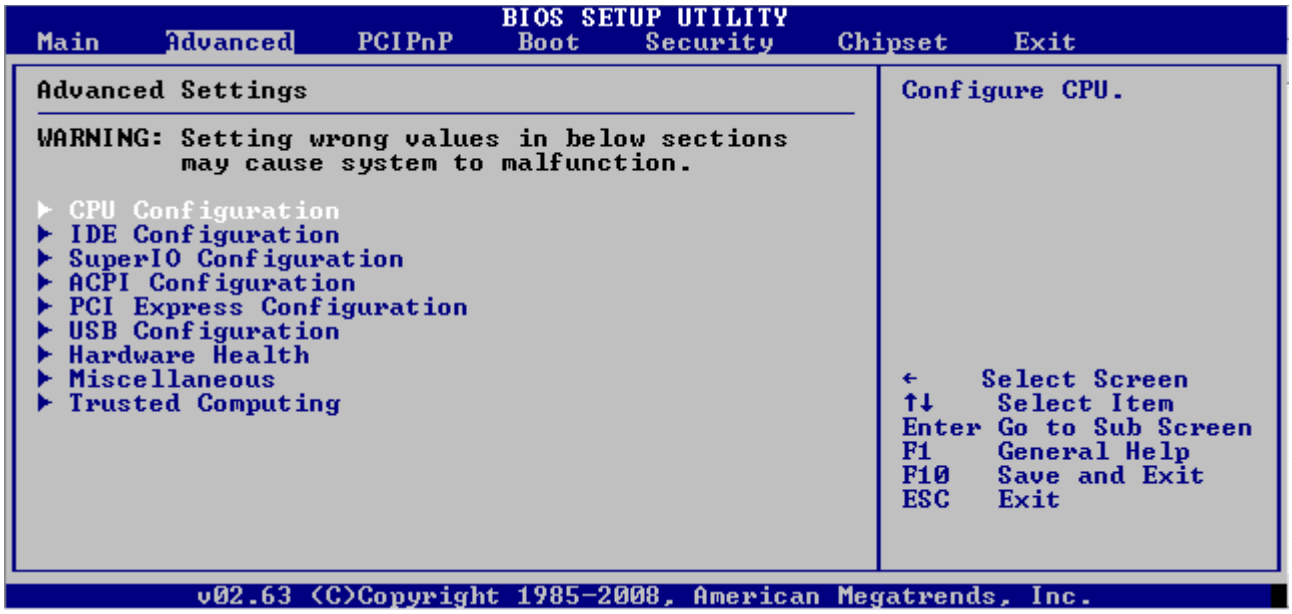
Module Software Revisions



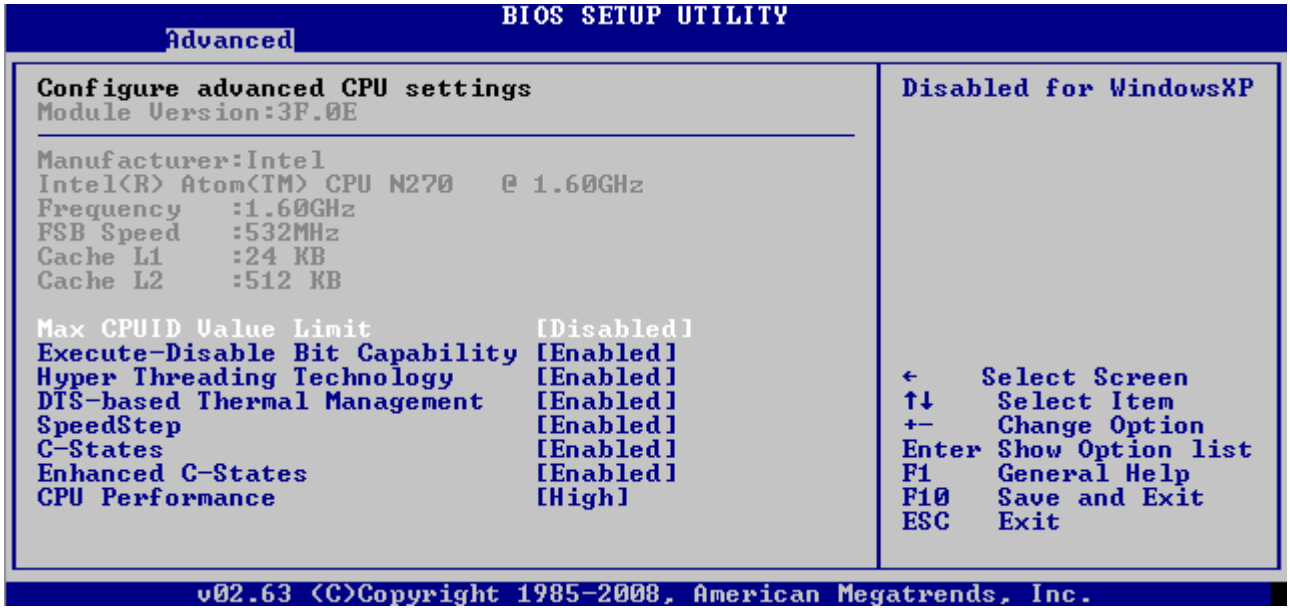
Current LVDS Configuration



7.4.3 Advanced Menu



CPU Configuration

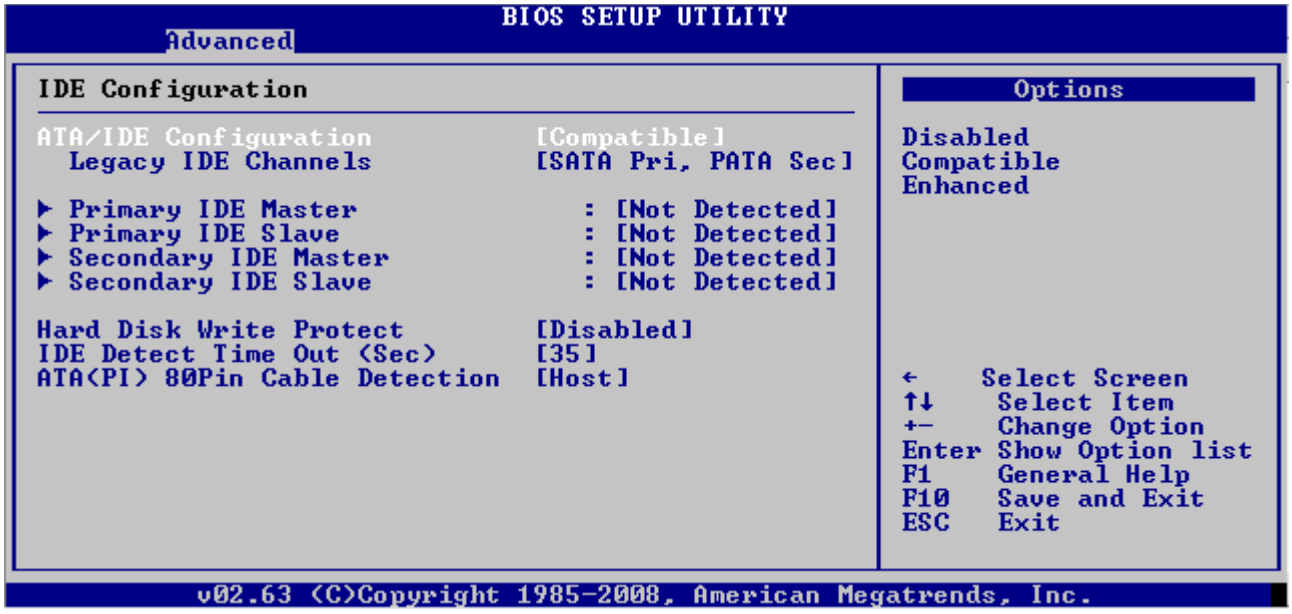


Feature	Option	Description
Max CPUID Value Limit	**Disabled** Enabled	Disabled for WindowsXP
Execute-Disable Bit Capability	**Enabled** Disabled	When disabled, force the XD feature flag to always return 0
Hyper Threading Technology	**Enabled** Disabled	Enable/Disable Hyper Threading Feature
DTS-based Thermal Management	**Enabled** Disabled	Enable/Disable Thermal Management utilizing the CPU's Digital Thermal Sensor
SpeedStep	**Enabled** Disabled	Enables and Disables the SpeedStep power management feature
C-States	**Enabled** Disabled	Enables and Disables the C - States.
Enhanced C-State Modes	**Enabled** Disabled	CPI idle is set to enhanced C-states, when enabled
CPU Performance	**High** Middle Low	Select CPU Performance after Post

CPU Performance Table

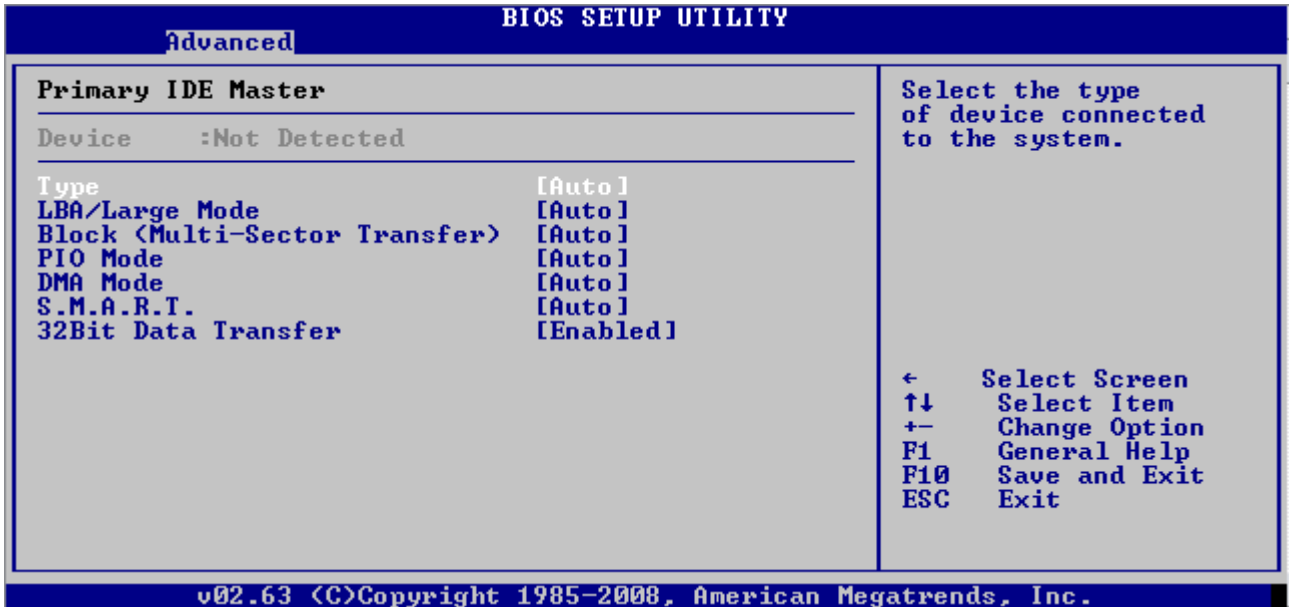
High	1600MHz
Middle	1200MHz
Low	800MHz

IDE Configuration



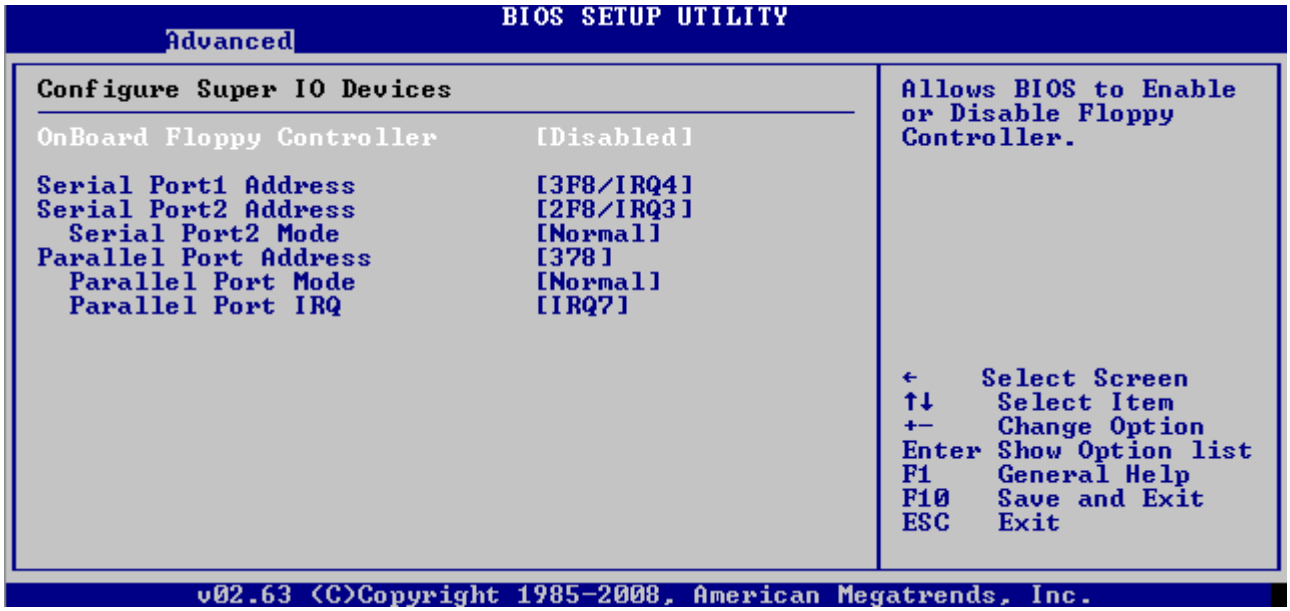
Feature	Option	Description
ATA/IDE Configuration	Disabled **Compatible** Enhanced	Disables or selects the mode for the ATA/IDE interface
Legacy IDE Channels	SATA only **SATA Pri, PATA Sec** PATA only	Selects the IDE channel behavior in compatible mode. (Only visible when IDE is configured to Compatible
Configure SATA# as	**IDE** AHCI	Selects the SATA mode in Enhanced IDE mode
Configure SATA# Channels	**Before PATA** Behind PATA	Configure when the SATA controller is initialized in Enhanced IDE mode
Hard Disk Write Protect	**Disabled** Enabled	Disables/enables device write protection. It will be effective only if device is accessed through BIOS functions.
IDE Detect Time Out (Sec.)	[0-35] **35**	Selects the time out value for the detection of ATA/ ATAPI devices
ATA(PI) 80Pin Cable Detection	Host & Device **Host** Device	Selects the mechanism for detecting 80Pin ATA(PI) cables.

IDE Device Submenu



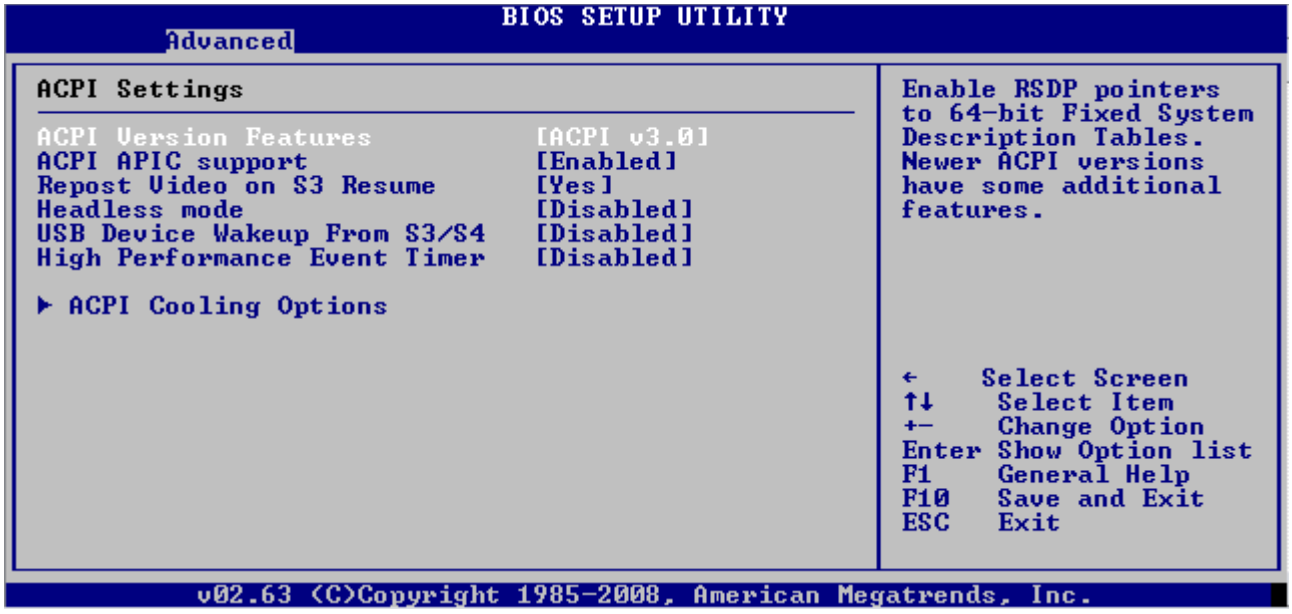
Feature	Option	Description
Type	Not Installed **Auto** CD/DVD ARMD	Selects the type of the IDE Devices connected to the system
LBA/Large Mode	Disabled **Auto**	Disables the LBA mode or enables it, when a device supports it
Block (Multi-Sector Transfer)	Disabled **Auto**	Disabled: The data transfer from and to the device occurs one sector ata atime Auto: The data transfer from and to the device occurs multiple sectors at a time if the device supports ist
PIO Mode	**Auto** 0 1 2 3 4	(Auto) Configures the PIO Mode
DMA Mode	**Auto** SWDMAn MWDMAn UDMAn	SWDMA: Single Word DMA MWDMA: Multi Word DMA UDMA: Ultra DMA
S.M.A.R.T.	**Auto** Enabled Disabled	Disables, Enables or automatically enables the S.M.A.R.T feature (Self-Monitoring, Analysis and Reporting Technology)
32Bit Data Transfer	**Enabled** Disabled	Disables and Enables the 32Bit Data Transfer Mode

SuperIO Configuration



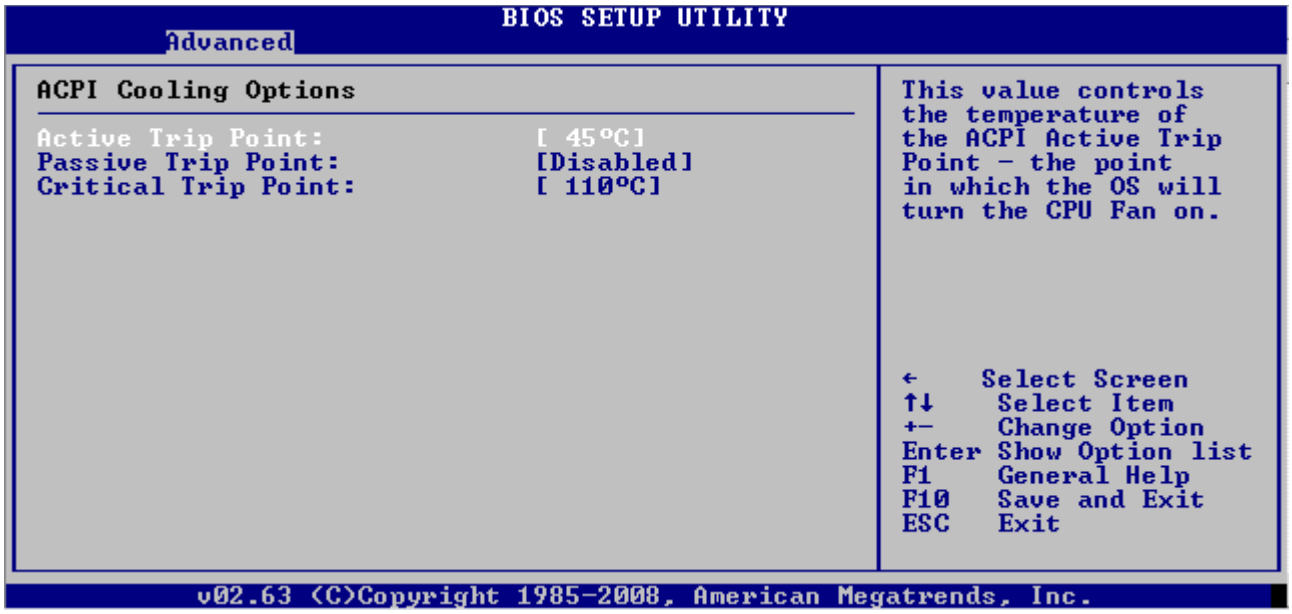
Feature	Option	Description
Onboard Floppy Controller	**Disabled** Enabled	Enables / Disables the floppy controller in BIOS
Serial Port1 Address	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Selects the Address of COM Port 1
Serial Port2 Address	Disabled 3F8/IRQ4 **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Selects the Address of COM Port 2
Serial Port2 Mode	**Normal** IrDA ASK IR	
Parallel Port Address	Disabled **378** 278 3BC	Selects the Address of the LPT Port
Parallel Port Mode	**Normal** Bi-Directional ECP EPP+SPP ECP+EPP	Allows BIOS to Select Parallel Port Mode. (Only visible when Parallel Port enabled.)
Parallel Port IRQ	IRQ5 **IRQ7**	Allows BIOS to Select Parallel Port IRQ. (Only visible when Parallel Port enabled.)

ACPI Settings



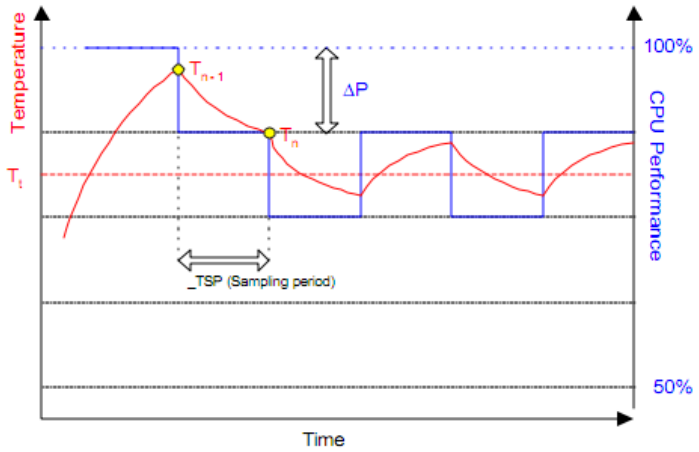
Feature	Option	Description
ACPI Version	**ACPI v.3.0** ACPI v.2.0 ACPI v.1.0	Selects the ACPI version
ACPI APIC support	**Enabled** Disabled	Include ACPI APIC table pointer to RSDT pointer list.
Repost Video on S3 Resume	No **Yes**	If yes, Videobios is reinitialized after S3 Resume
Headless Mode	**Disabled** Enabled	Enables / Disables headless mode through ACPI
USB Device Wakeup From S3/S4	**Disabled** Enabled	Enables / Disables the possibility to wake up via USB from S3 and S4
High Performance Event Timer	**Disabled** Enabled	Enables / Disables the High Performance Event Timer
HPET Memory Address	**FED00000h** FED01000h FED02000h FED03000h	Selects the Address of the High Performance Event Timer, when enabled.

ACPI Cooling Options



Feature	Option	Description
Active Trip Point	Disabled 40°C **45°C** 50°C ... 110°C	This value controls the temperature of the ACPI Active Trip Point - the point in which the OS will turn the CPU fan on.
Passive Trip Point	**Disabled** 40°C 45°C 50°C ... 110°C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the CPU.
Passive TC1 value	**1** 2 3 ... 16	This value sets the TC1 value for the ACPI Passive Cooling Formula. (Only visible when Passive Trip Point is enabled.)
Passive TC2 value	1 2 ... **5** ... 16	This value sets the TC2 value for the ACPI Passive Cooling Formula. (Only visible when Passive Trip Point is enabled.)
Passive TSP value	2 4 ... **10** ... 30	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when Passive Cooling is Enabled.
Critical Trip Point	Disabled 40°C 45°C 50°C ... **110°C**	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut off the system.

Passive Cooling



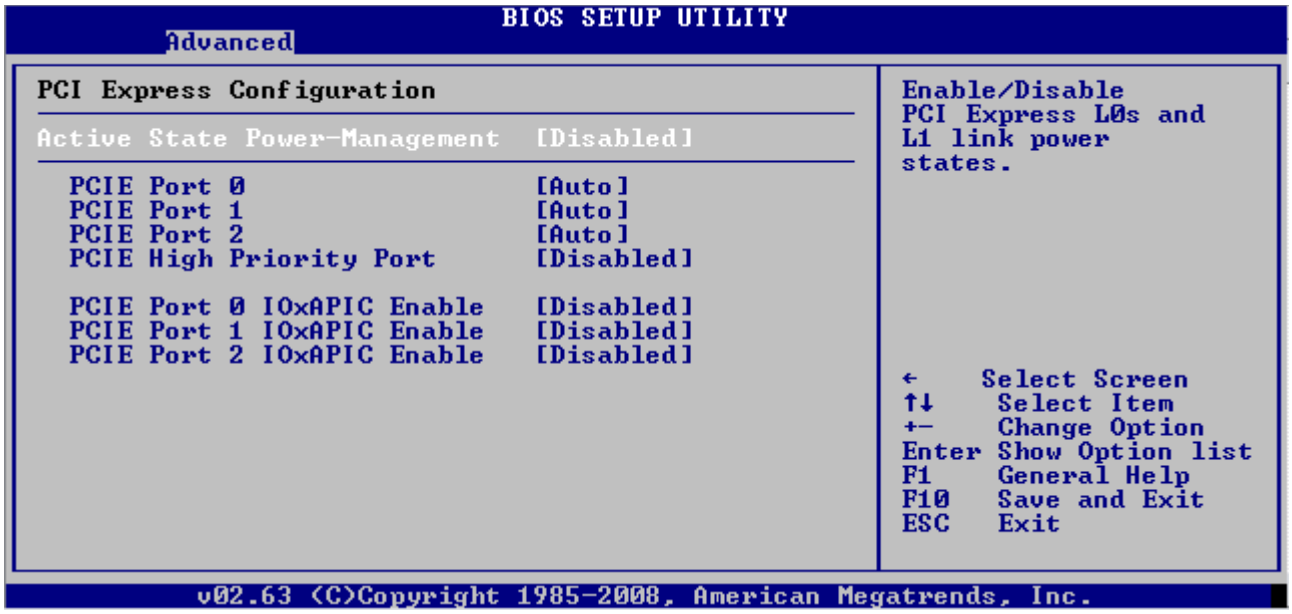
The ACPI OS assesses the optimum CPU performance change necessary to lower the temperature using the following equation

?P[%] = TC1 (Tn-Tn-1) + TC2 (Tn-Tt)

?P is the performance delta, Tt is the target temperature = passive cooling trip point. The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants the end user must supply. It's up to the end user to set the cooling preference of the system by setting the appropriate trip points in the BIOS setup.

See chapter 12 of the ACPI specification (www.acpi.info) for more details

PCI Express Configuration

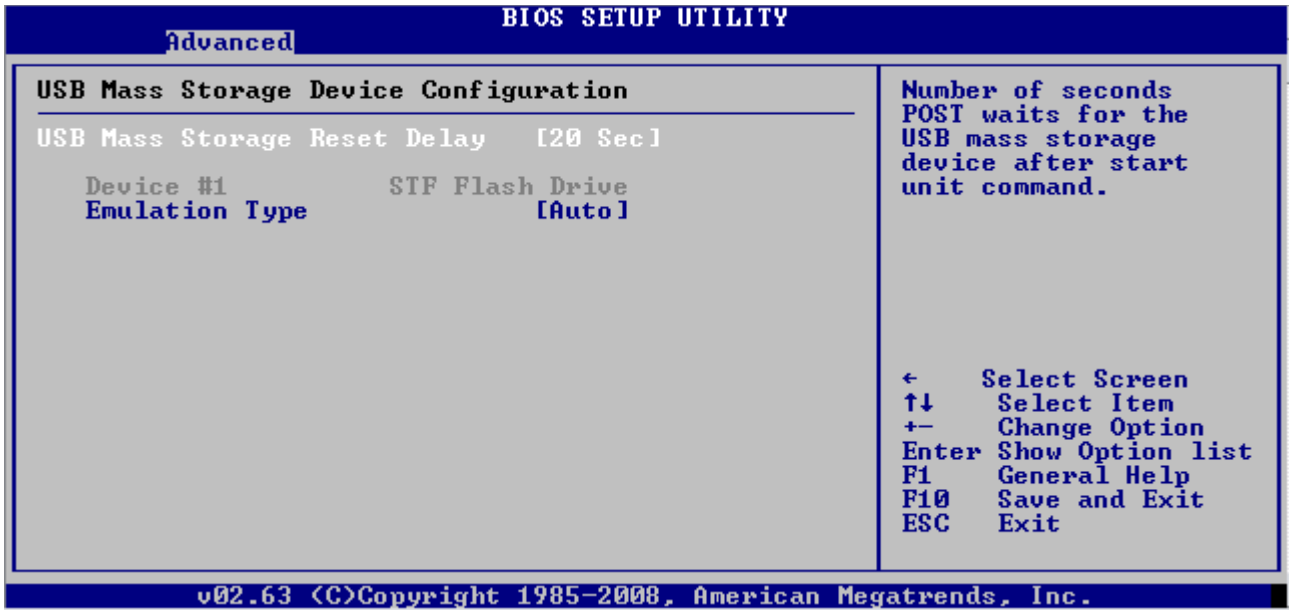


Feature	Option	Description
Active State Power Management	**Disabled** Enabled	Enables/Disables PCI Express L0 and L1 link power states.
PCIE Port N	**Auto** Enabled Disabled	Enables/Disables or autoconfigures the PCIE Port N
PCIE High Priority Port	**Disabled** Port 0 Port 1 Port 2 ... Port 5	Select the PCIE Port that gets higher priority than the others.
PCIE Port N IOxAPIC Enable	**Disabled** Enabled	Enables/Disables the APIC Support for the PCIE Port N

USB Configuration

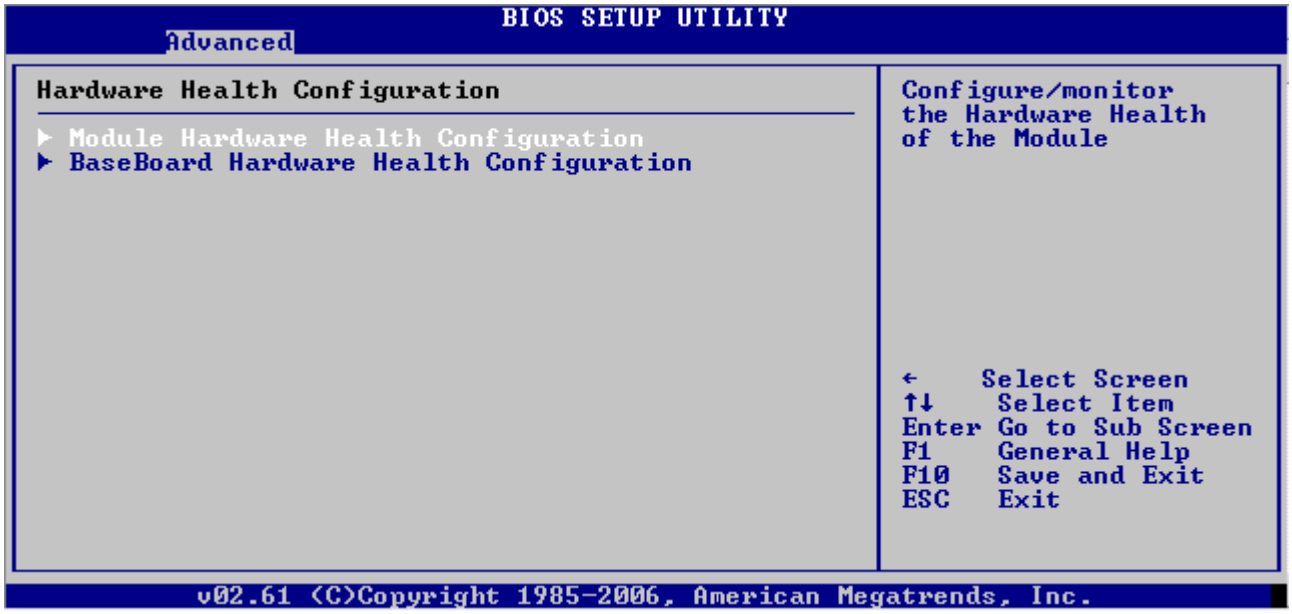
Feature	Option	Description
Legacy USB Support	Auto Disabled **Enabled**	Enables support for legacy USB. Auto option disables legacy support if no USB devices are connected.
Port 64/60 Emulation	Disabled **Enabled**	Enables IO port 60h/64h emuluation support.
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps)
BIOS EHCI Hand-Off	Disabled **Enabled**	This is a workaround for an OS without EHCI hand-off support. The EHCI ownership change should claim by the EHCI driver
USB reset delay	**Disabled** Enabled	Enables extra delay after reset during USB initialization.

USB Mass Storage Device Configuration

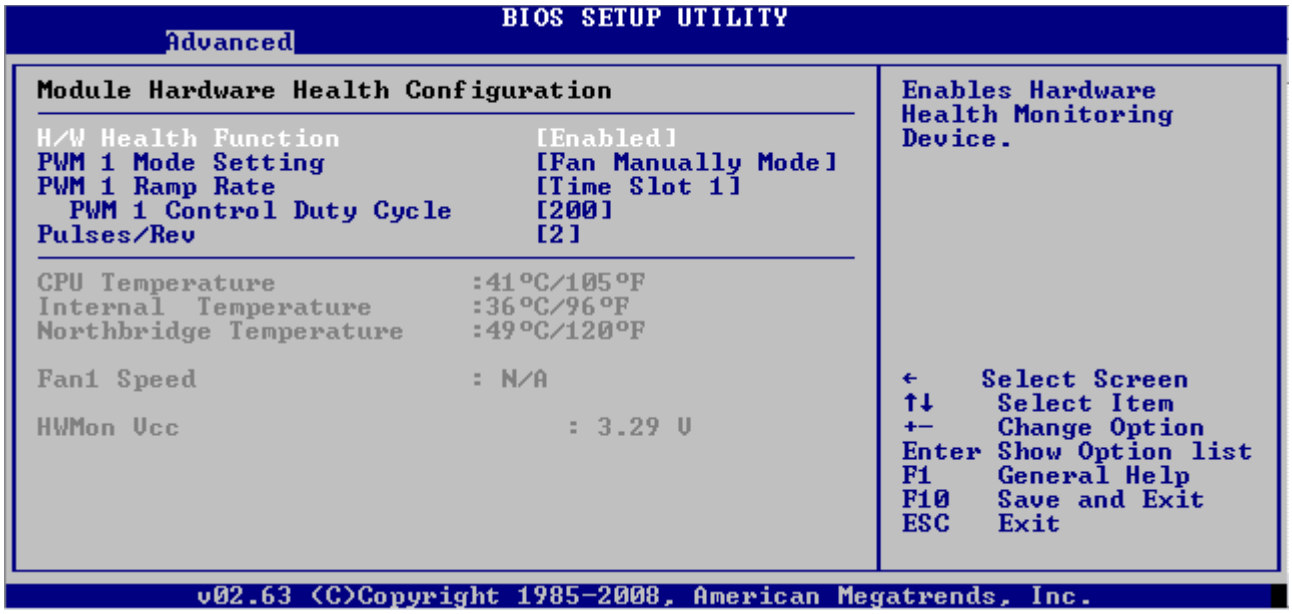


Feature	Option	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto USB devices with less than 530MB will be emulated as floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

Hardware Health

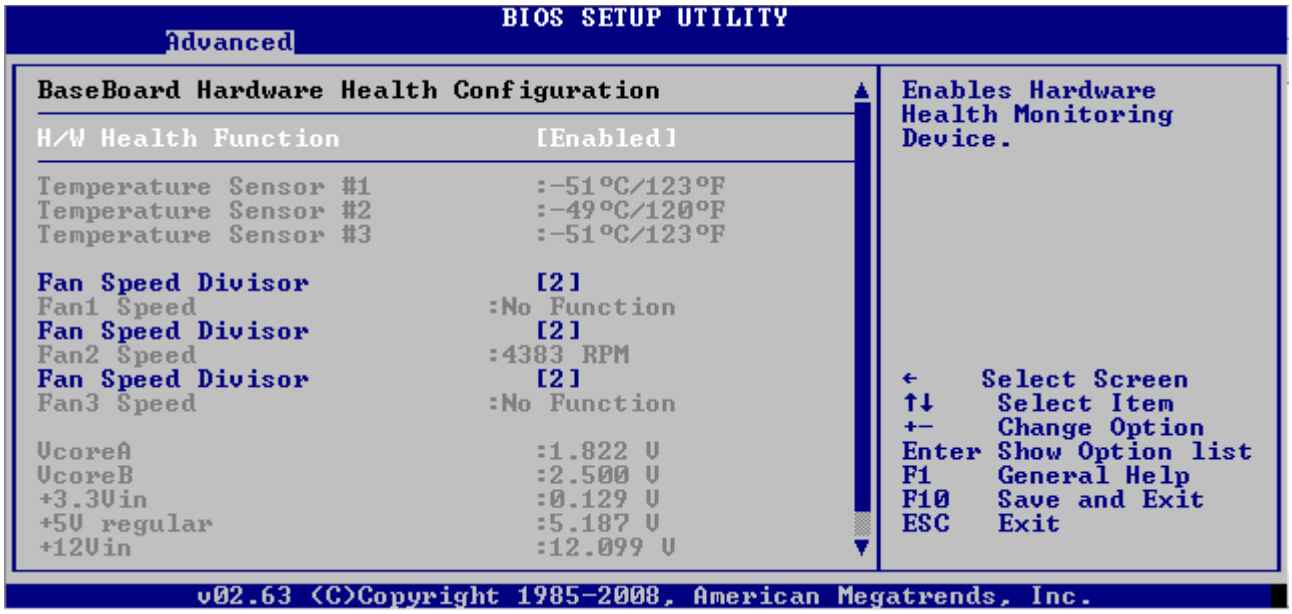


Module Hardware Health



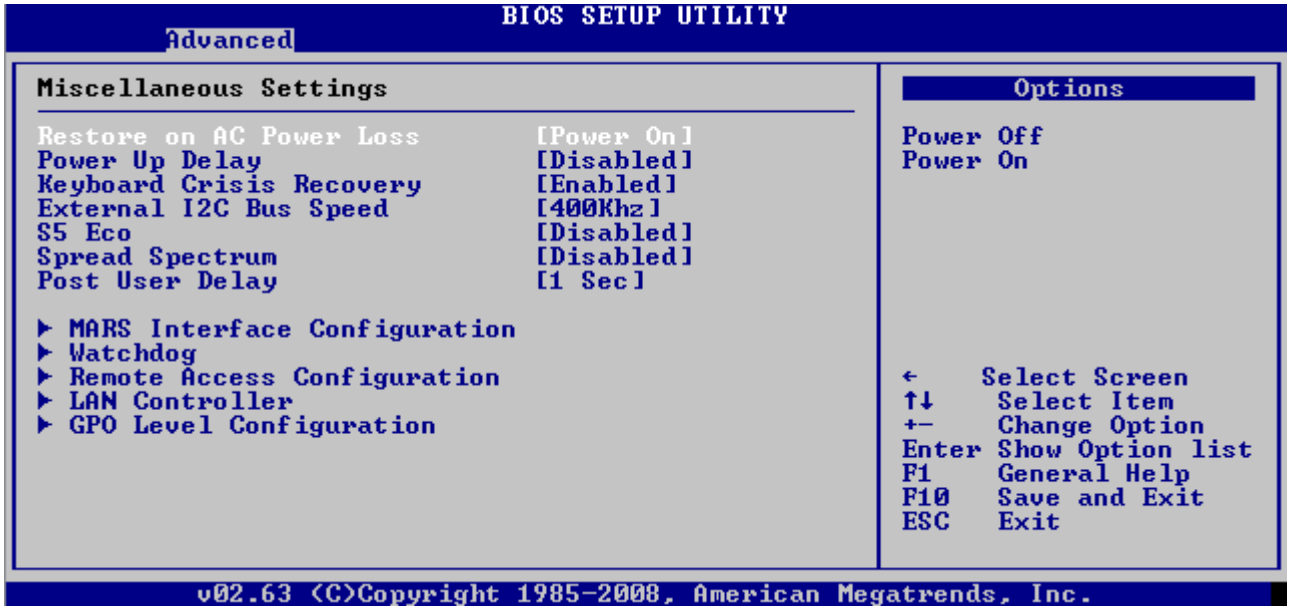
Feature	Option	Description
H/W Health Function	Disabled **Enabled**	Enables Hardware Health Monitoring Device.
PWM 1 Mode Setting	Auto Fan Mode Fan Always On Full Fan Disable Mode **Fan Manually Mode**	PWM Configuration Mode Setting
PWM 1 Ramp Rate	**Time Slot 1** Time Slot 2 Time Slot 3 Time Slot 4 Time Slot 8 Time Slot 12 Time Slot 24 Time Slot 48	
PWM 1 Control Duty Cycle	[0...255] **200**	Controls the length of a PWM duty cycle.
Pulses/Rev	[1...4] **2**	

Baseboard Hardware Health



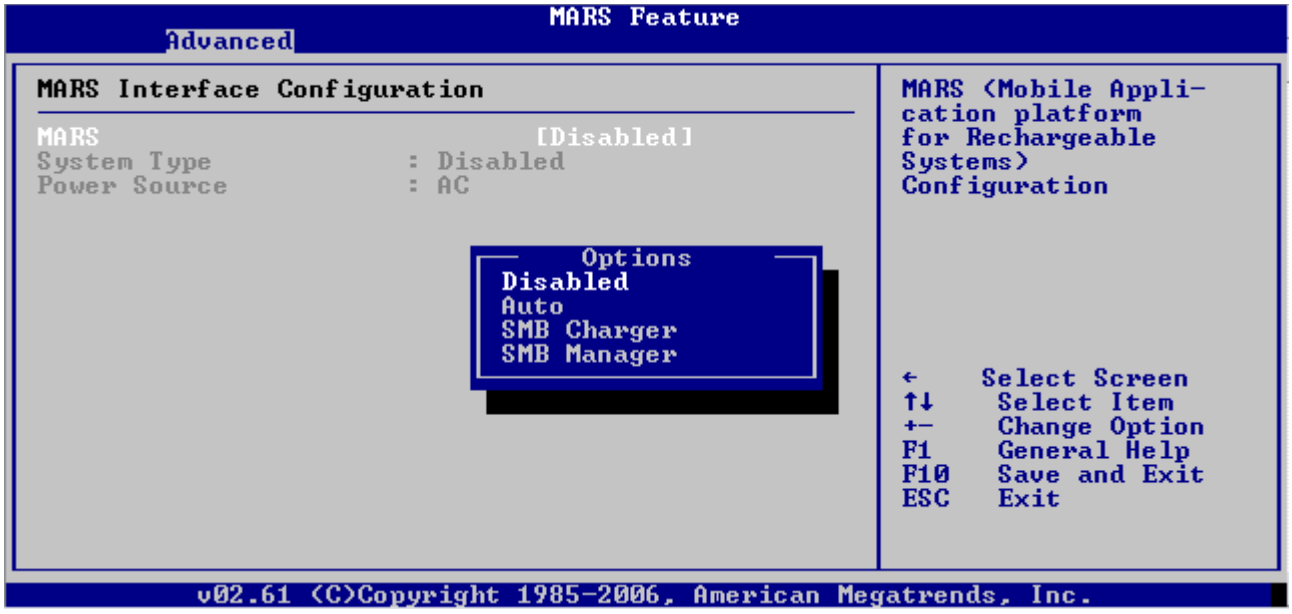
Feature	Option	Description
H/W Health Function	**Disabled** Enabled	Enables Hardware Health Monitoring Device.
Fan Speed Devisor 1	1 **2** 4 ... 128	Sets the register setting for the baseboard windbond fan speed devisor for fan 1
Fan Speed Devisor 2	1 **2** 4 ... 128	Sets the register setting for the baseboard windbond fan speed devisor for fan 2
Fan Speed Devisor 3	1 **2** 4 ... 128	Sets the register setting for the baseboard windbond fan speed devisor for fan 3

Miscellaneous Settings



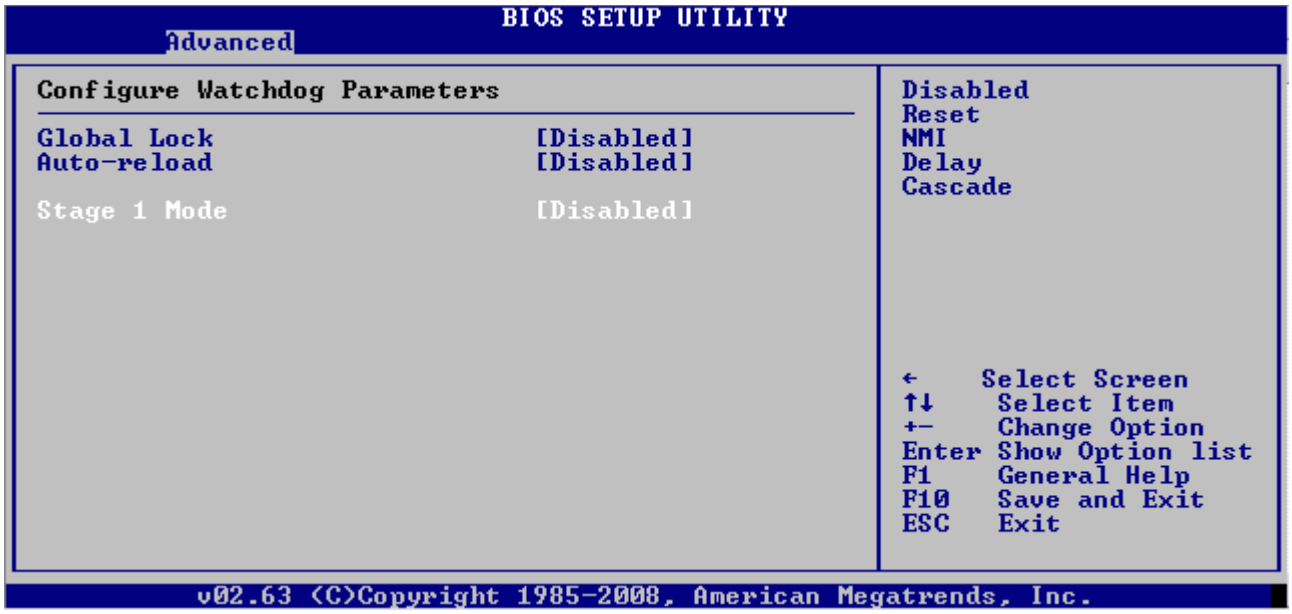
Feature	Option	Description
Restore on AC Power Loss	Power Off **Power On**	Controls the behavior after Power Loss in ATX mode
Power Up Delay	**Disabled** 4 to 5 seconds 3 to 4 seconds 2 to 3 seconds 1 to 2 seconds	Delay after power up, when in an G3 cycle
Keyboard Crisis Recovery	Disabled **Enabled**	Enables/Disables Keyboard Crisis Recovery function by USB keyboard
External I2C Bus Speed	800Khz **400Khz** 200Khz ... 1Khz	Selects the Speed of the I2C bus interface
S5 Eco	**Disabled** Enabled	Enables/Disables S5 Eco Mode to reduce supply current in soft off (S5). See manual for usage of S5 Eco.
Spread Spectrum	**Disabled** PCI CPU both	Enalbes/Disables Spread Spectrum for the selected clocks.
Post User Delay	None **1 Sec** 2 Sec ... 10 Min	Delay during POST

MARS Interface Configuration



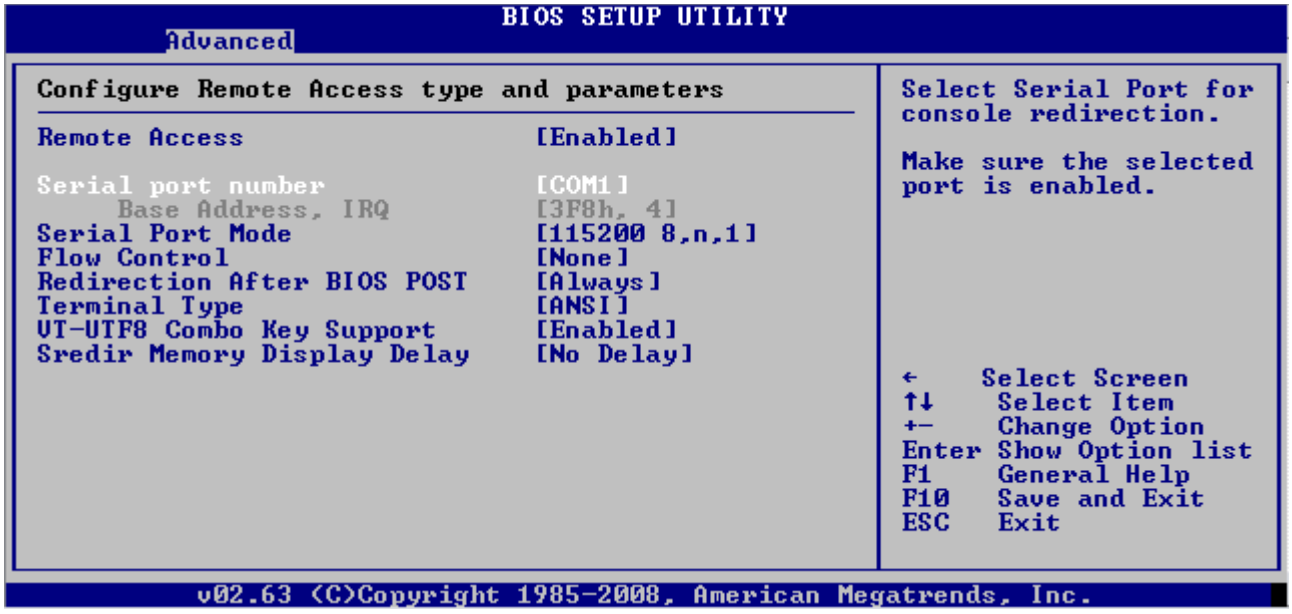
Feature	Option	Description
MARS	**Disabled** Auto SMB Charger SMB Manager	Enables the MARS function

Watchdog



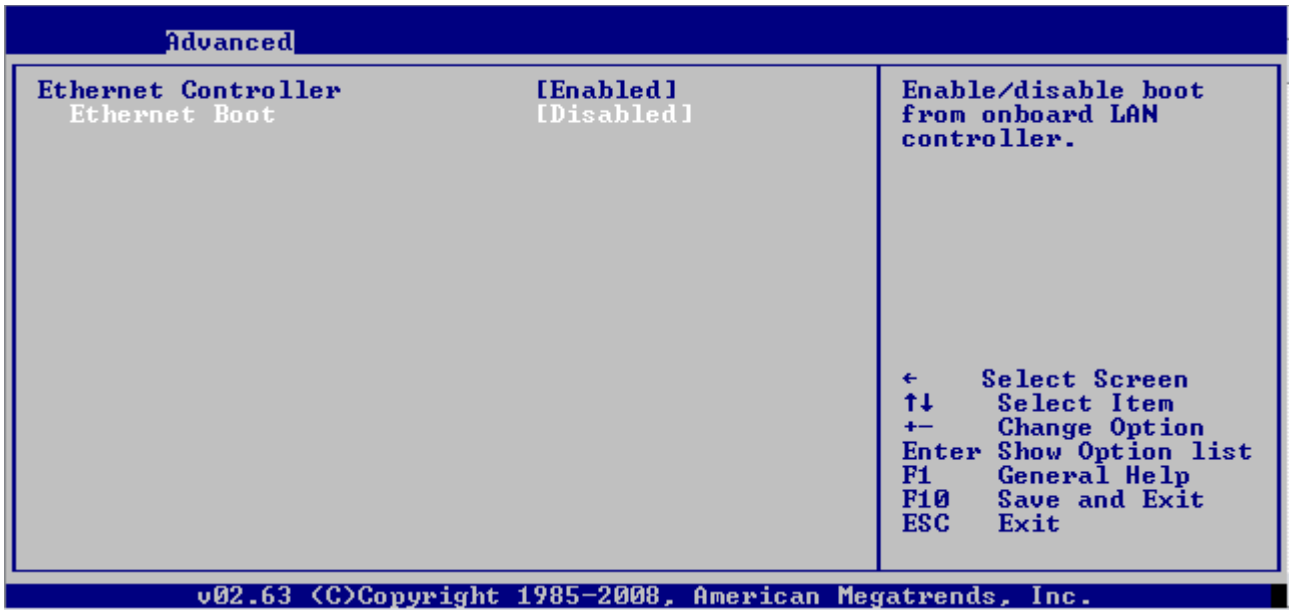
Feature	Option	Description
Global Lock	**Disabled** Enabled	If set to enabled all Watchdog registers (except WD_KICK) become read only
Auto-reload	**Disabled** Enabled	If set to enable the watchdog timers will be automatically reloaded at timeout
Stage 1 Mode	**Disabled** Reset NMI Delay Cascade	Selects the mode of the first stage Reset: resets the module NMI: activates an non maskable interrupt Delay: set a time to wait once during boot up Cascade: without action, used every retrigger
Assert WDT	**Disabled** Enabled	Enable/disable assertion of WDT signal to baseboard on stage timeout
Stage 1 Timeout	**0.4s** 1s 5s 10s 30s 1:00m 5:00m 10:00m	Controls the timeout of the 1st watchdog stage
Stage 2 Mode	**Disabled** Reset NMI	Selects the mode of the 2nd stage Reset: resets the module NMI: activates an non maskable interrupt
Assert WDT	**Disabled** Enabled	Enable/disable assertion of WDT signal to baseboard on stage timeout
Stage 2 Timeout	**0.4s** 1s 5s 10s 30s 1:00m 5:00m 10:00m	Controls the timeout of the 1st watchdog stage

Remote Access Configuration



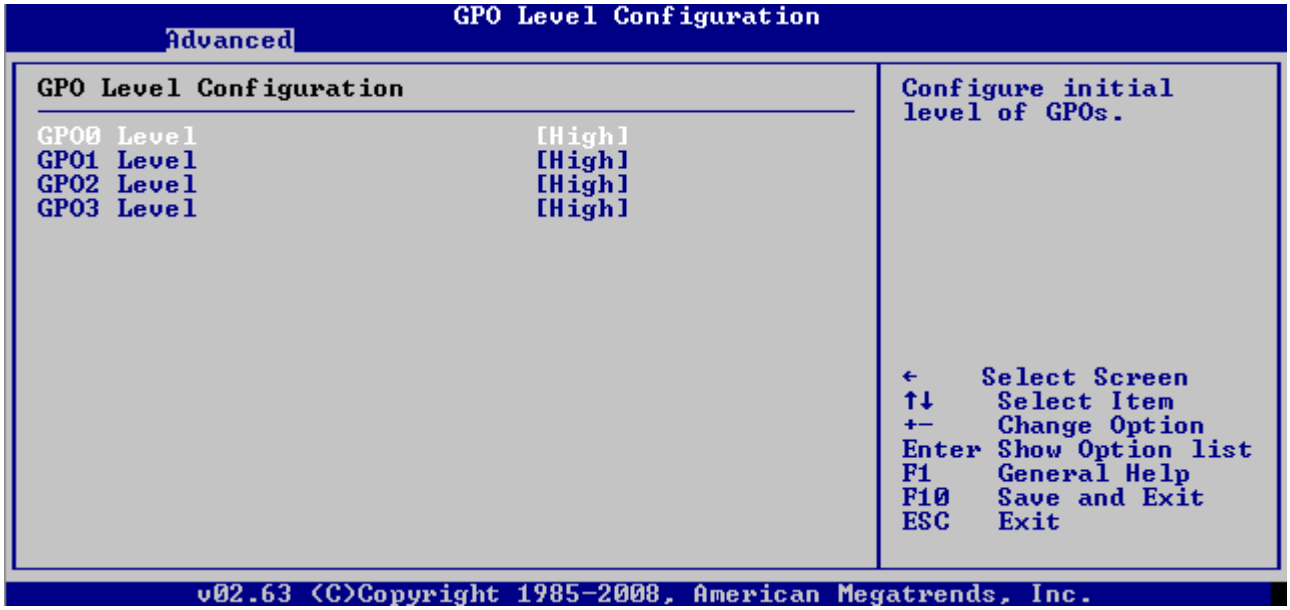
Feature	Option	Description
Remote Access	**Enabled** Disabled	Enables Remote Access via AMI Console Redirection
Serial port number	COM1	Select serial port for console redirection, selectable ports must be enabled
Serial port Mode	**115200 8,n,1** 57600 8,n,1 28400 8,n,1 19200 8,2,1 09600 8,n,1	Select serial port mode for console redirection
Flow Control	**none** Hardware Software	Selects the flow control for serial connection
Redirection After BIOS POST	**Always** Disabled Bootloader	Always: Redirection is always active Disabled: Turns off after POST Bootloader: Turns off after bootloader
Terminal Type	**ANSI** VT100 VT-UTF8	Select the target terminal type
VT-UTF8 Combo Key Support	**Enabled** Disabled	Enables VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Sredir Memory Display Delay	**No Delay** Delay 1 Sec Delay 2 Sec Delay 4 Sec	Enables Remote Access via AMI Console Redirection

LAN Controller



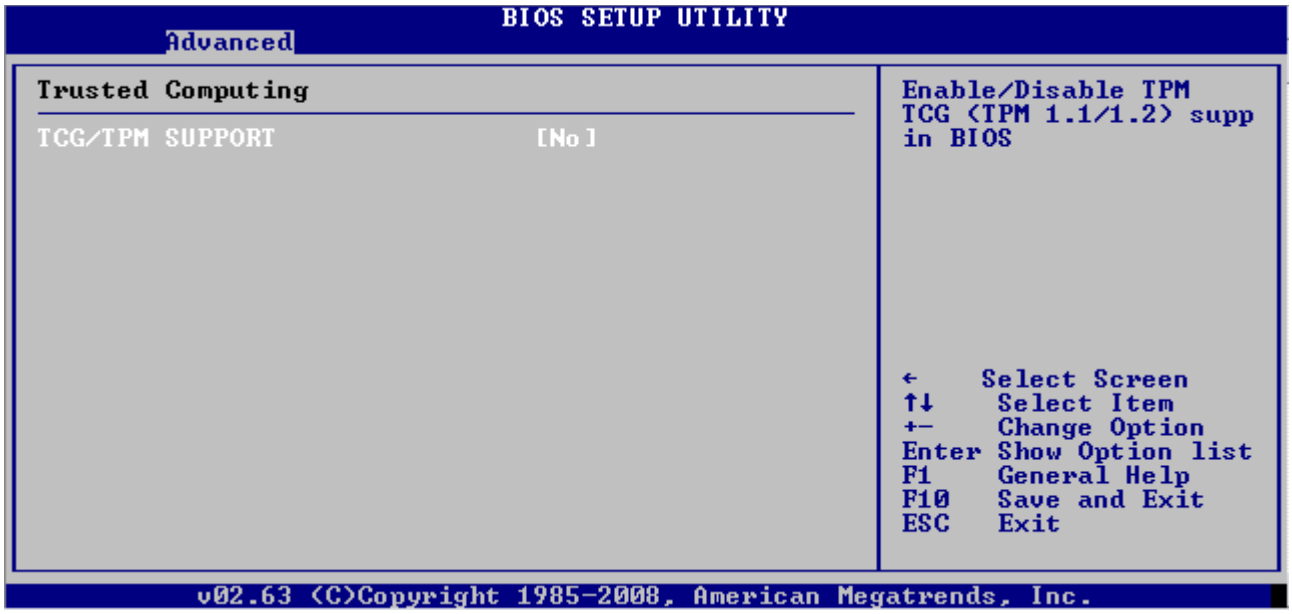
Feature	Option	Description
Ethernet Controller	Disabled **Enabled**	Disables / Enables the onboard Ethernet interface
Ethernet Boot	**Disabled** Enabled	Disables / Enables the PXE Boot ROM

GPIO Level Configuration



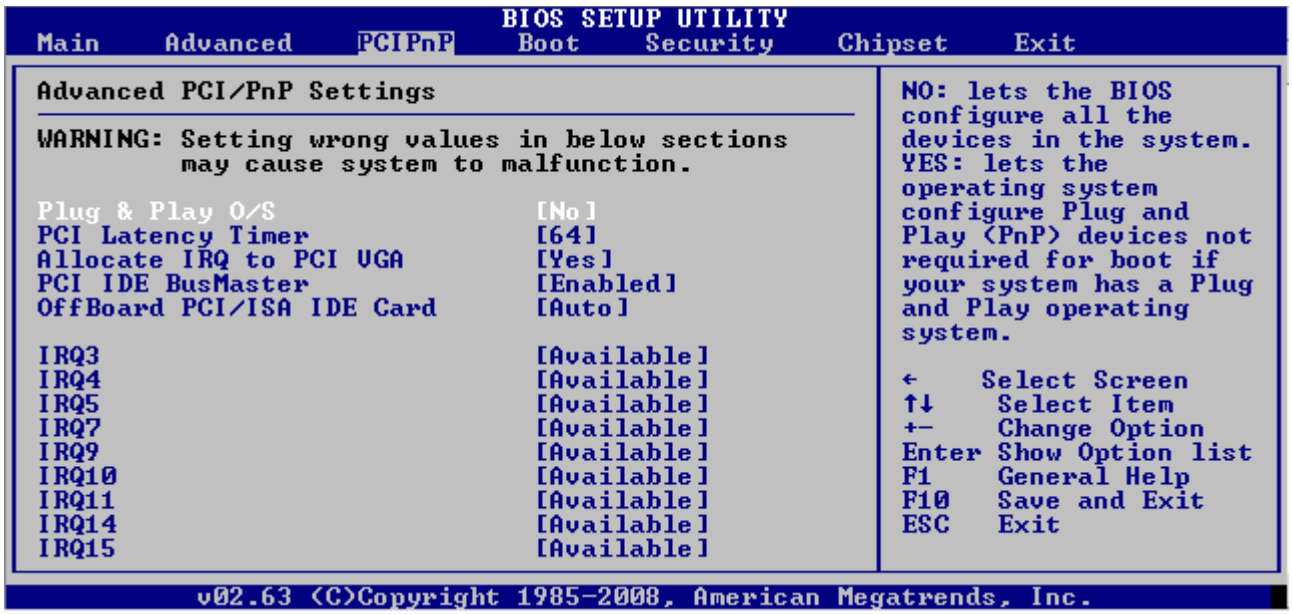
Feature	Option	Description
GPO0 Level GPO1 Level GPO2 Level GPO3 Level	Low **High**	Configure initial level of GPOs

Trusted Computing



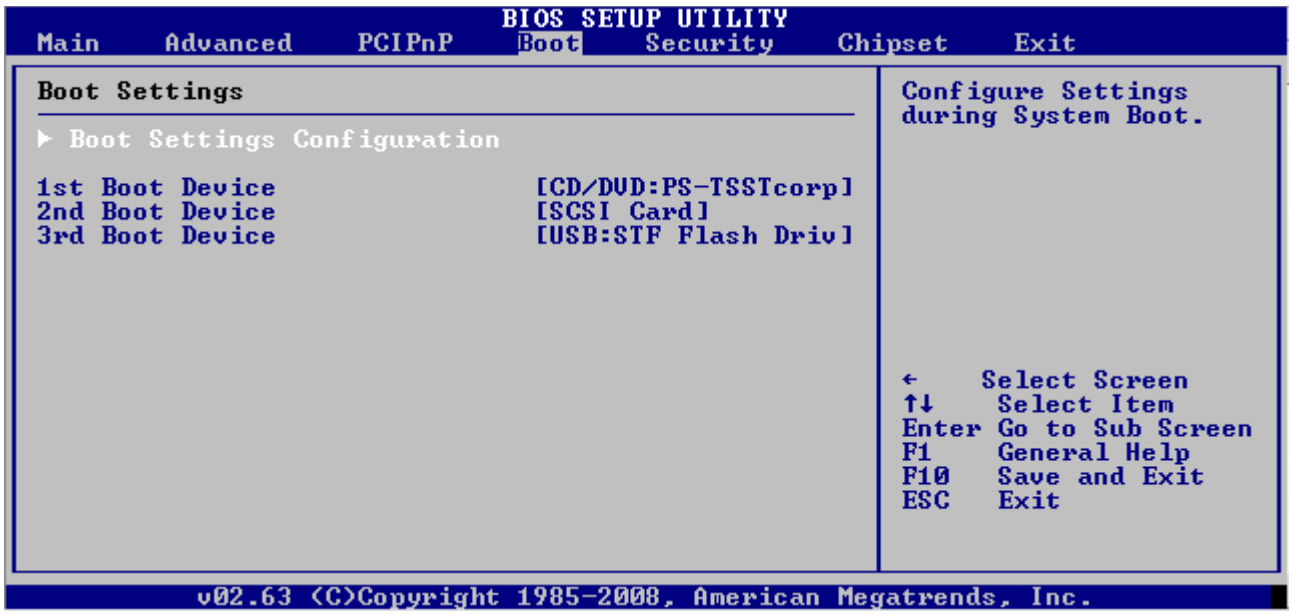
Feature	Option	Description
TCG/TPM Support	Yes **No**	Enables / Disables Trusted Computing and Trusted Platform Module

7.4.4 PCIPnP Menu



Feature	Option	Description
Plug & Play O/S	**No** Yes	No: all devices are initialized by BIOS Yes: OS has to initialize some devices
PCI Latency Timer	32 **64** ... 248	Value in units of PCI clocks for PCI device latency register
Allocate IRQ to PCI VGA	**Yes** No	Decided if PCI VGA card does get an IRQ assigned if requested
PCI IDE BusMaster	Disabled **Enabled**	Disables and enables PCI IDE Busmaster
OffBoard PCI/ISA IDE Card	**Auto** PCISlot 1 PCISlot 2 ... PCISlot 6	Some IDE Cards needs this , with set to Auto it works with most cards
IRQ3 ... IRQ15	**Available** Reserved	Available: IRQ useable by PCI/PnP devices Reserved: IRQ is reserved for ISA devices

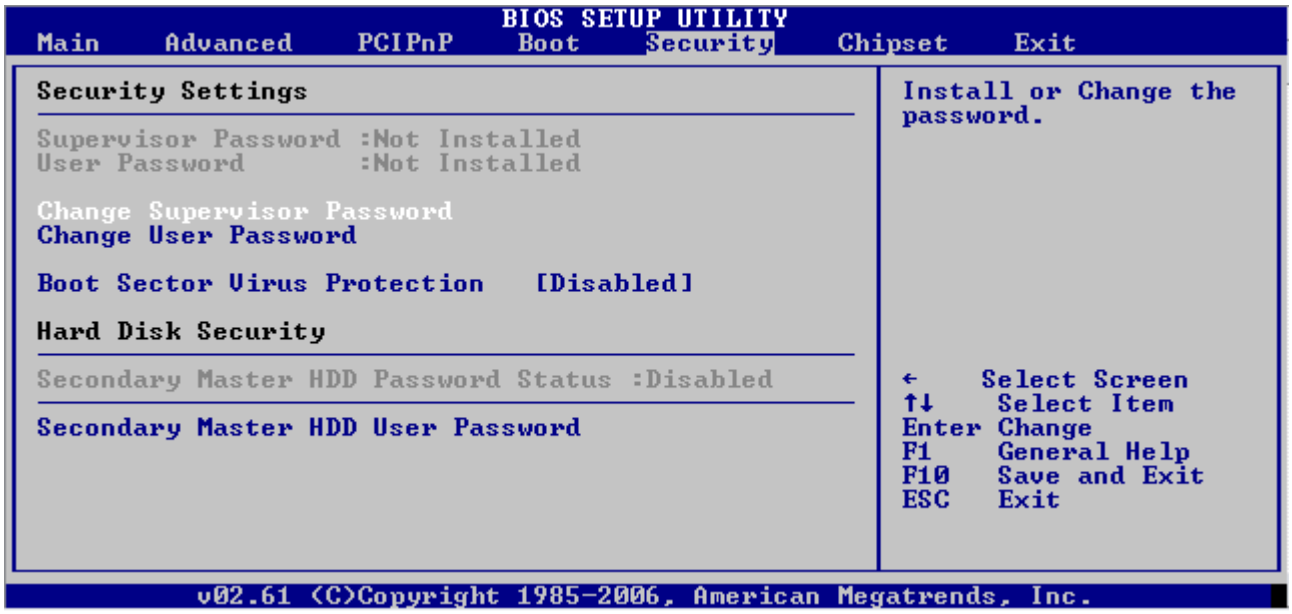
7.4.5 Boot


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Boot Settings
Boot Settings Configuration
1st Boot Device [CD/DVD:PS-TSSTcorp]
2nd Boot Device [SCSI Card]
3rd Boot Device [USB:STF Flash Driv]
Configure Settings during System Boot.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
v02.63 (C)Copyright 1985-2008, American Megatrends, Inc.

Boot Setting Configuration

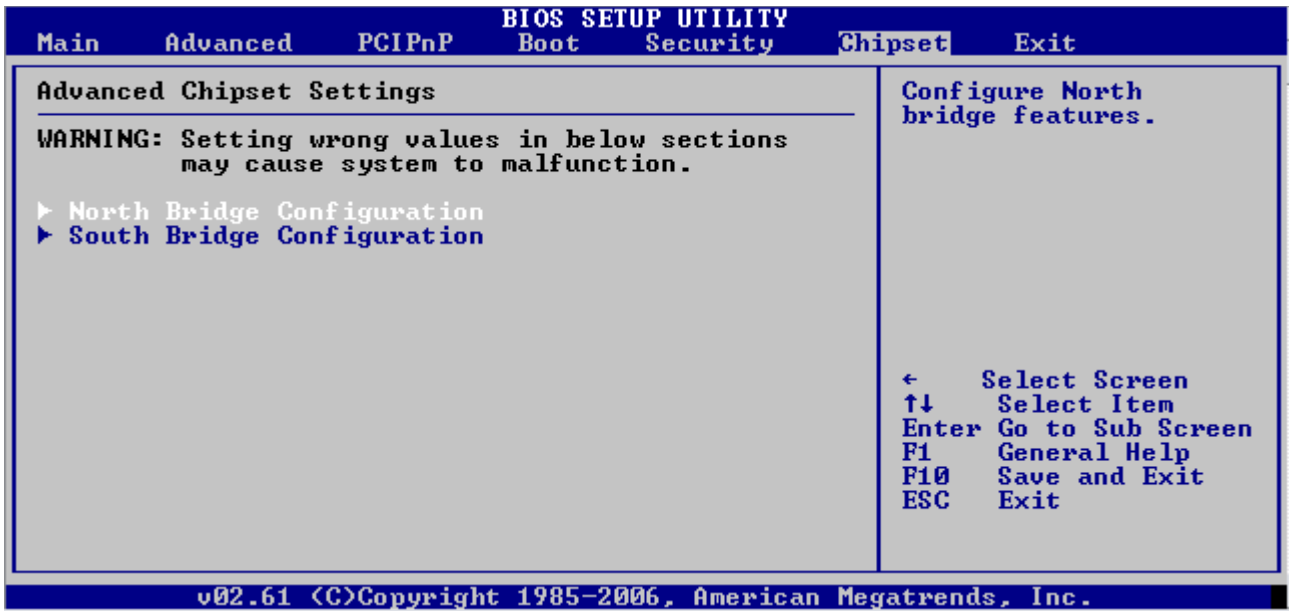
Feature	Option	Description
Quick Boot	**Enabled** Disabled	Disables or enables the quick boot feature
Quiet Boot	**Disabled** Enabled	Disabled: Shows normal POST messages Enabled: Shows OEM Logo during boot up
AddOn ROM Display Mode	**Force BIOS** Keep Current	Set Display Mode for Option ROM
Bootup Num-Lock	**On** Off	Select Power-On state for Num-Lock
PS/2 Mouse Support	**Auto** Disabled Enabled	Disables and enables or auto selects PS/2 Mouse Support
Wait For 'F1' If Error	**Disabled** Enabled	Wait for F1 key to be pressed, if error
Hit 'DEL' Message Display	**Enabled** Disabled	Displays: “Hit 'DEL' to run setup” during POST, if enabled
Boot USB HDD first	**Disabled** Enabled	If enabled, boots new attached USB HDD always first
Interrupt 19 Capture	**Disabled** Enabled	Allows option ROMs to trap INT19h if enabled

7.4.6 Security



Feature	Option	Description
Change Supervisor Password	**Type in**	
Change User Password	**Type in**	
Boot Sector Virus Protection	**Disabled** Enabled	Enables or disables boot sector virus protection.

7.4.7 Chipset


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Advanced Chipset Settings
WARNING: Setting wrong values in below sections
may cause system to malfunction.
North Bridge Configuration
South Bridge Configuration
Configure North bridge features.
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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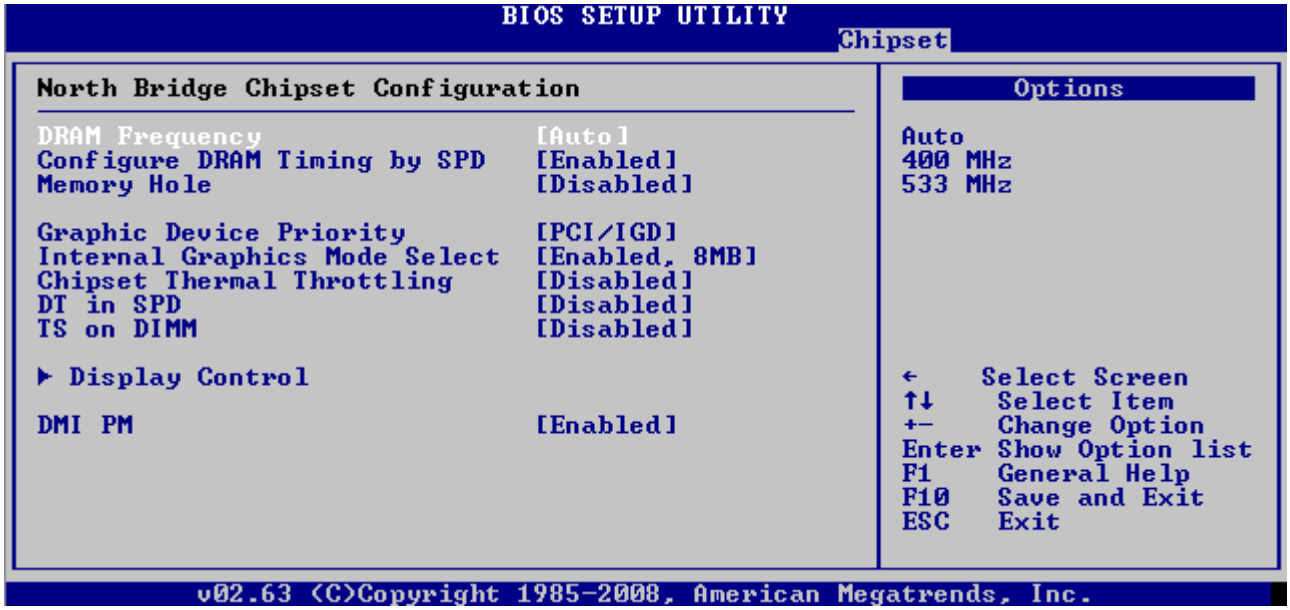
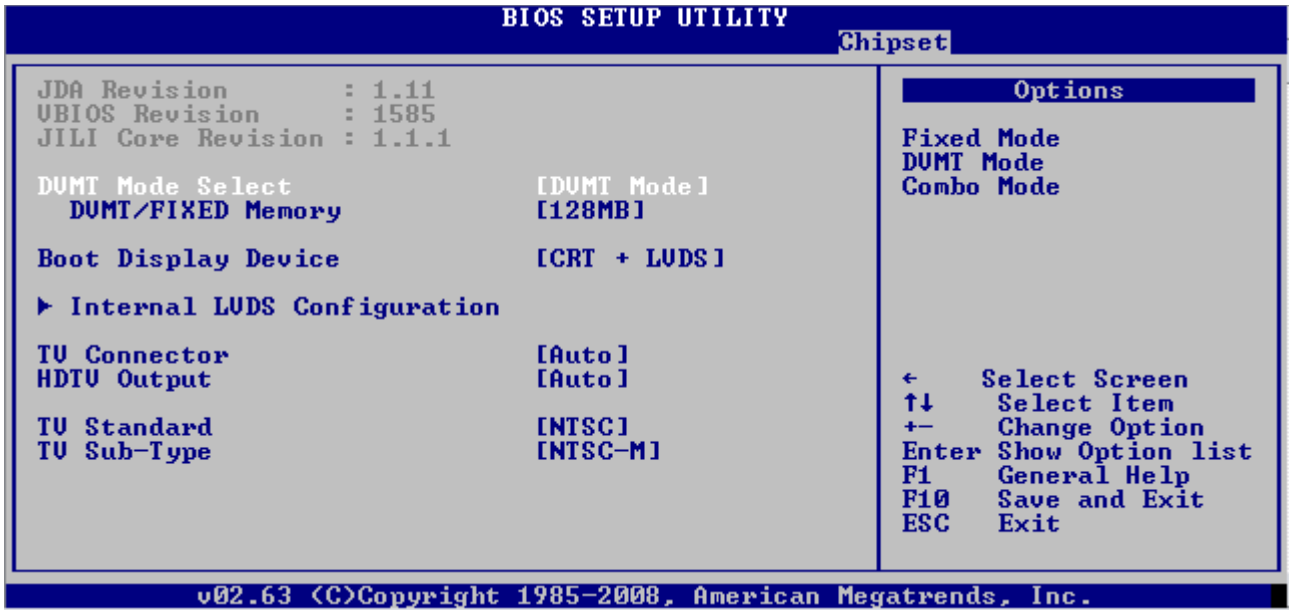
North Bridge Configuration



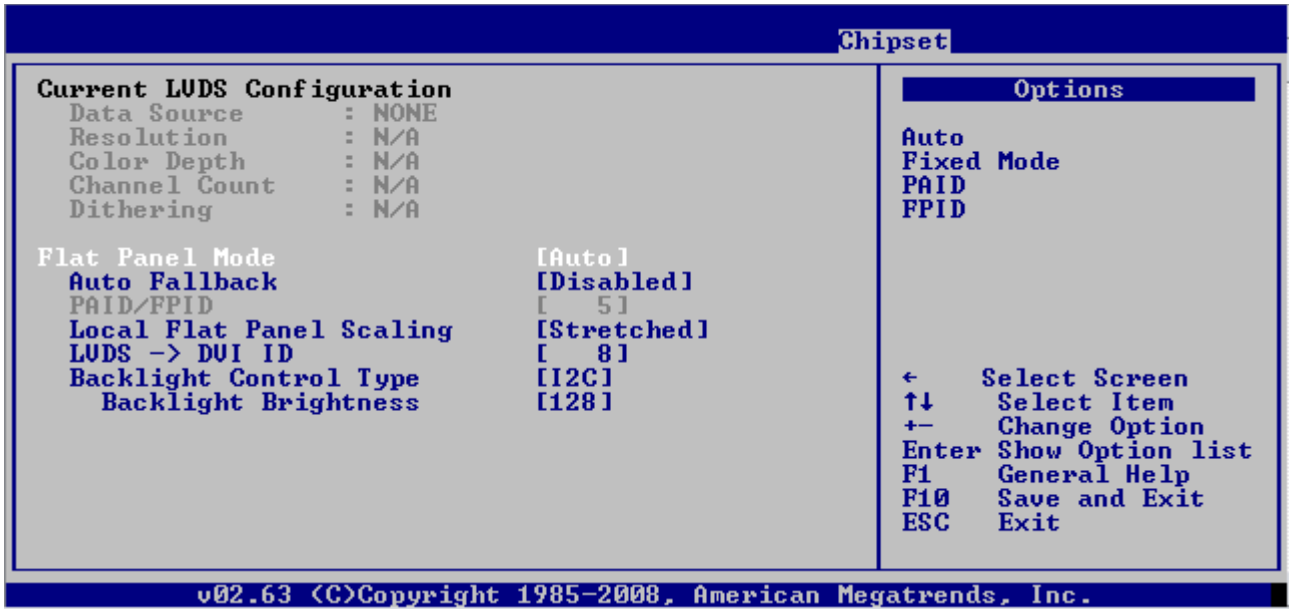
Feature	Option	Description
DRAM Frequency	**Auto** 400Mhz 533Mhz	Selects the DRAM frequency
Configure DRAM Timing by SPD	Disabled **Enabled**	Disables and Enables automatic DRAM configuration via SPD EEPROM
Memory Hole	**Disabled** 15MB-16MB	Disables and Enables the incredible useless extended memory hole
Graphic Device Priority	IGD PCI/IGD	Selects which graphics adapter is initialized during boot up and gets priority
Internal Graphics Mode Select	Disabled Enabled, 1MB **Enabled, 8MB**	Select the mode for the interal graphicdevice
Chipset Thermal Throttling	**Disabled** Enabled	Disables and Enables Chipset Thermal Throttling.
DT in SPD	**Disabled** Enabled	The GMCH supports the Delta Temperature (DT) in SPD thermal managmeent algorithm as specified by JEDEC.
TS on DIMM	**Disabled** Enabled	Disables and Enables the Thermal Sensor on DIMM.
DMI PM	Disabled **Enabled**	Disables or Enables DMI/FSB power management. If disabled, PCI performance will improve slightly.

Display Control



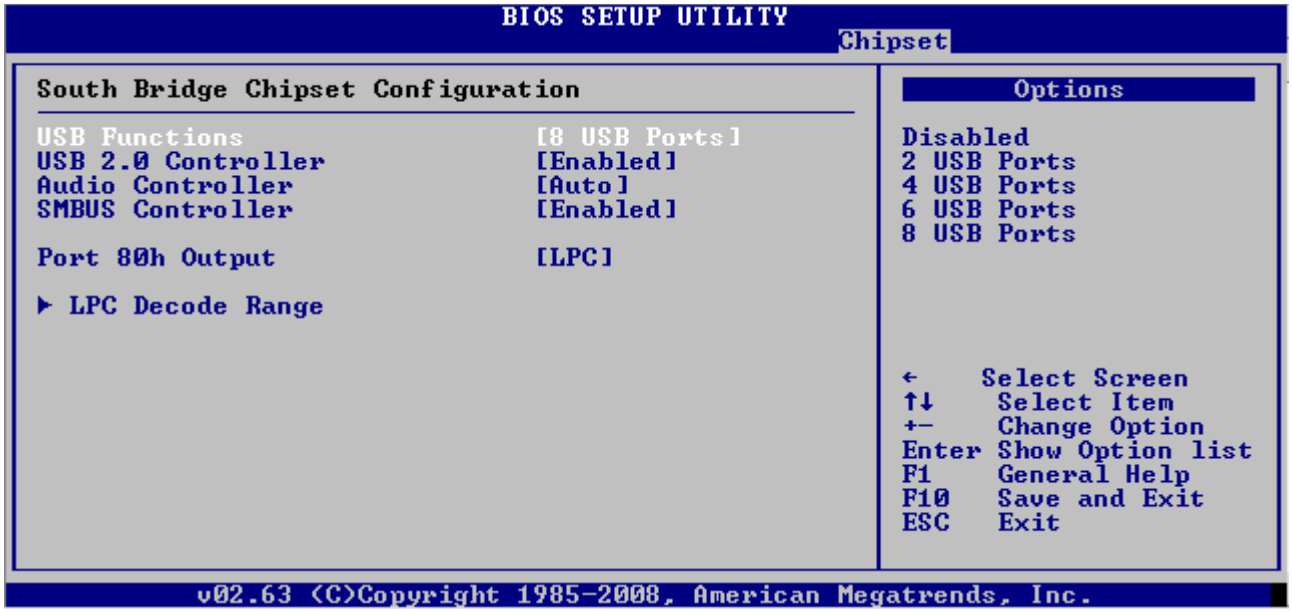
Feature	Option	Description
DVMT Mode Select	Fixed Mode **DVMT Mode** Combo Mode	Selects the Mode for Dynamic Video Memory Technology
DVMT/FIXED Memory	64MB **128MB** \Max DVMT	Configures the amount of memory for the Dynamic Video Memory Technology
Boot Display Device	CRT TV SDVO CRT+SDVO LVDS **CRT+LVDS**	Selects the Boot Display Devices
TV Connector	**Auto** Composite Component Composite & RGB S-Video SCART Composite SCART Compos. & RGB SCART Compos. & S-Video SMPTE253 Compon. RGB	Selects the TV Connector Type
HDTV Output	**Auto** 480i60 ... 1080p60	Selects the HDTV Output Mode
TV Standard	**NTSC** PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	Selects the regarding TV standard for TV out interface
TV Sub-Type	Depending on TV Standard	Selects the regarding TV Sub-Type

Internal LVDS Configuration



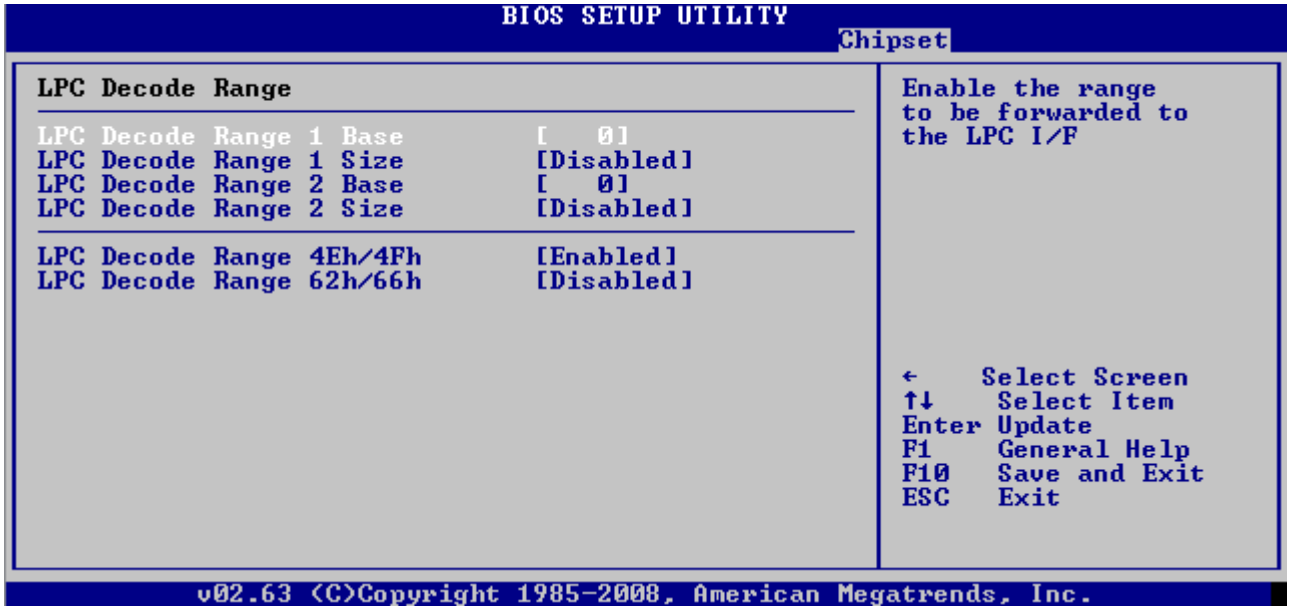
Feature	Option	Description
Flat Panel Mode	**Auto** Fixed Mode PAID FPID	Selects the Mode for the flat panel detection
Auto Fallback	**Disabled** Fixed Mode	Selects what happens, when there is no EEPROM detected (only when FPM: Auto)
Flat Panel Type	**VGA 640×480** … WXGA 1280×800	Selects the resolution of the LVDS display (only in FMP: Fixed Mode)
PAID/FPID	[X]	Selects the number of the PAID/FPID
Channels	**Single Channel** Dual Channel	Selects, if 1x or 2x LVDS signals are used (only in FPM: Fixed Mode)
Color Depth	**18bit**	Selects the Color Depth of the connected LVDS display (only in FPM: Fixed Mode)
Dithering	**Enabled**	Selects what happens, when there is no EEPROM detected (only when FPM: Auto)
Local Flat Panel Scaling	Centered **Stretched** Disabled	Selects the Scaling Options for the LVDS panel (only in FPM: Fixed Mode)
LVDS → DVI ID	5 **8**	Please Type In! 5 = 1×18 8 = 2×18
Backlight Control Type	None/External **I2C** PWM	Selects the mode for Backlight Control
Backlight Brightness	[0…255]	Selects the default setting for Backlight Brightness

Southbridge Configuration



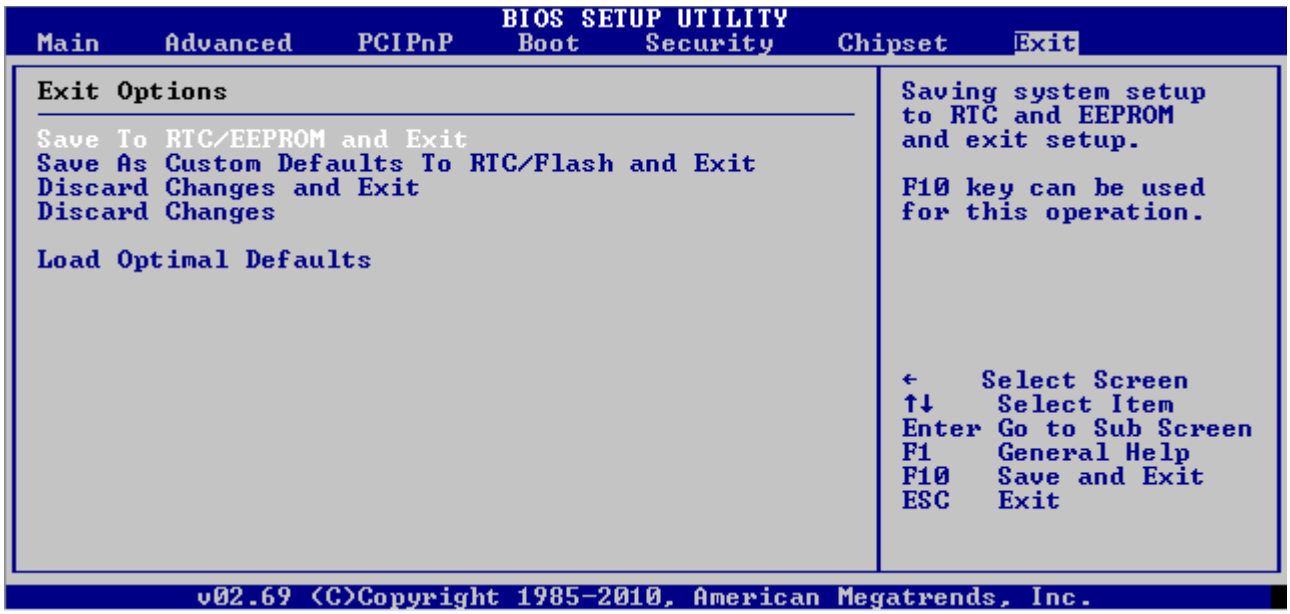
Feature	Option	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports ... **8 USB Ports**	Enables / Disables USB ports
USB 2.0 Controller	**Enabled** Disabled	Enables / Disables the USB 2.0 controller.
Audio Controller	**Auto** Azalia AC'97 Audio und Modem All Disable	Selects the mode for Audio Controller
SMBUS Controller	**Enabled** Disabled	Enables / Disables the SMBus controller
Port 80h Output	**LPC** PCI	Selects the Inteface for Port 80h output during POST

LPC Decode Range



Feature	Option	Description
LPC Decode Range 1 Base	[0...FFFF]	Enter the Base Adress of the LPC decode range
LPC Decode Range 1 Size	**Disabled** 4 8 ... 256	Size of the decode range in kB
LPC Decode Range 2 Base	[0...FFFF]	Enter the Base Adress of the LPC decode range
LPC Decode Range 2 Size	**Disabled** 4 8 ... 256	Size of the decode range in kB
LPC Decode Range 4Eh/4Fh	**Enabled** Disabled	Enables disables the LPC decode range at 4Eh/4Fh
LPC Decode Range 62h/66h	**Disabled** Enabled	Enables disables the LPC decode range at 62h/66h

7.4.8 Exit Menu



Corporate Offices

Europe, Middle East & Africa
Oskar-von-Miller-Str. 1
85386 Eching/Munich
Germany
Tel.: +49 (0)8165/ 77 777
Fax: +49 (0)8165/ 77 219
info@kontron.com

North America
14118 Stowe Drive
Poway, CA 92064-7147
USA
Tel.: +1 888 294 4558
Fax: +1 858 677 0898
info@us.kontron.com

Asia Pacific
17 Building,Block #1,ABP.
188 Southern West 4th Ring
Beijing 100070, P.R.China
Tel.: + 86 10 63751188
Fax: + 86 10 83682438
info@kontron.cn